Title: MEMS-Electronics Integration: A Smart Temperature Sensor for an Organ-on-a-chip Platform

Authors: Ronaldo Martins da Ponte, Vasiliki Giagka, Wouter A. Serdijn

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In this work, an *in-situ* smart temperature sensor is designed and monolithically integrated in an organ-on-a-chip (OOC) platform. This will allow a non-incubator temperature monitoring, besides a more accurate temperature measurement of the cell culture.

The custom, simple, robust and flexible IC technology used for the sensor fabrication grants a very cost-effective integrated solution in virtue of the reduced cost per wafer along with the large silicon area available in the platform.

The circuit comprises a PTAT generator that periodically feeds a current controlled oscillator to produce a digitally-represented signal. The temperature information depends on this feeding periodicity, therefore, it is encoded in the time domain. The periodic switching activity is controlled by the output of the comparator and the first buffer stage. The output can be interfaced with a microcontroller for further post-processing.

The fabrication used a “MEMS-last” process to avoid potential PDMS and other material contamination. A planar BiCMOS IC technology that requires only 7 masks steps is used to fabricate NPN and n/p-MOSFET transistors. A double-polished p-type silicon wafer was used. Mask 1 defines the n-well and the collector area of the NPN transistor, while masks 2 and 3 define, respectively, the n/p-type diffusion areas for the CMOS and the emitter/base area for the bipolar device. Contact openings are wet etched after the patterning of mask 4, while mask 5 is used to pattern the interconnect and gate material via deposition of AlSi. Masks 6 and 7 are used to open vias and deposit the second metallization. This last step is also used to deposit the first metallization of the OOC. The process follows with the SiO_2 deposition using PECVD on the front and back of the wafer. The SiO_2 layer on the back is dry etched to define the membrane area. PDMS is spun onto the front of the wafer and cured for 30 min at 90 °C. Finally, the membrane is released removing the Si and the SiO_2 layers from underneath the membrane using DRIE and BHF, respectively. Wafer level measurements confirms the functionality of the circuit.

Title: A Switched Capacitor DC-DC Buck Converter for a Wide Input Voltage Range

Authors: Alessandro Urso, Wouter A. Serdijn

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In this work, a power-efficient multiphase Recursive Switched Capacitor (RSC) converter is presented.

Conventionally, RSC converters are used to obtain many different output voltages from a fixed input voltage.

Here, the converter provides a fixed output voltage of 1 V at 1 mA from an input voltage ranging from 1.4 V to 4.5 V. It has one programmable stage (2:1 or 3:2) followed by four 2:1 stages. Contrary to most conventional topologies, depending on the input voltage, not all the stages are always deployed. This allows to increase the power efficiency of the whole architecture. The flying capacitance of the non-activated stages is transferred to the activated ones. Hence, for any given input voltage, 100 % of the on-chip capacitance is always used for the conversion.

For a general 2:1 topology, an analytical analysis of the power losses is carried out and the impact of the overdrive voltage of the switches on the power efficiency is quantified.

where it will shown how the overdrive voltage of the switches impact the power efficiency.

A novel gate-driver technique for the switches involved in the conversion is proposed. It ensures an

optimal overdrive voltage of the transistor, irrespective of its source and drain potentials.
The 16-phase interleaved converter employs a charge recycling technique and uses a total on-chip capacitance of 3 nF.
The RSC converter is designed to be implemented in a standard 40 nm CMOS process which offers a capacitor density of approximately 2 nF/mm^2. Circuit simulations over the whole input voltage range show a power efficiency never lower than 54 % with a peak value of 92.7 %.

Title: High-Pass ΣΔ Converter Design Using a State-Space Approach and Its Application to Cardiac Signal Acquisition
Authors: Sampi Rout, Wouter A. Serdijn
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Cardiac signal acquisition with high linearity and accuracy of the high-pass cut-off frequency imposes a challenge on the implementation of the analog preprocessing and the analog-to-digital converter. A state-space based design methodology is proposed to develop HP sigma-delta ADC topologies, targeting high accuracy of the high-pass cut-off frequency and good linearity. By using the state-space synthesis approach, sigma-delta converters with arbitrary signal and quantization noise transfer functions can be synthesized. State-space techniques allow dynamic range optimization of the sigma-delta converters with respect to signal swing and noise through state and noise scaling, respectively. This also minimizes the sensitivity of the topology to component variations. A sensitivity performance analysis of the noise transfer function with respect to integrator non-idealities and coefficient variations is also described. Intermediate functions are evaluated mathematically to compare the proposed HP sigma-delta topologies with respect to dynamic range. From the intermediate-function analysis, it is seen that the noise from the high-pass integrator is low-pass filtered. Also, from the L2-norm calculations, it is observed that the orthonormal HP sigma-delta ADC gives better noise performance than the observable HP sigma-delta ADC. Finally, schematic simulations of a circuit designed in AMS 0.18 um CMOS IC technology verify the findings and match the system level results. The designed orthonormal HP sigma-delta achieves a linearity of 11.02 bits and the accuracy of the high-pass cut-off is better than 1%. It is also tested with a real pre-recorded ECG input signal and successfully reduces baseline wandering.