Towards CMOS Bulk Sensing for *In-Situ* Evaluation of ALD Coatings for Millimeter Sized Implants

Kambiz Nanbakhsh, Riina Ritasalo, Wouter A. Serdijn, and Vasiliki Giagka

***Abstract*— To meet the dimensional requirements for bioelectronic medicine, new packaging solutions are needed that could enable small, light-weight and flexible implants. For protecting the implantable electronics against biofluids, recently various atomic layer deposited (ALD) coatings have been proposed with high barrier properties. Before implantation, however, the protective coating should be evaluated for any defects which could otherwise lead to leakage and device failure. In these cases, the conventional helium leak test method can no longer be used due to the millimeter size of the implant. Therefore, an *in-situ* sensing platform is needed that could evaluate the coating and justify the implantation of the final device. In this work, we explore the possibility of using the CMOS bulk for such a platform. Towards this aim, as a proof of concept, test chips were made in a standard 6-metal 0.18 µm CMOS process and for the connection to the bulk, a p+ diffusion was used. A group of samples was then coated with an ALD multilayer. For coating evaluation, off-chip DC current leakage and impedance measurements were carried out in saline between the CMOS bulk and a platinum reference electrode. Results were compared between non-coated and coated chips that clearly demonstrated the potential of using the bulk as a sensing platform for coating evaluations. This novel approach could pave the way towards an all integrated *in-situ* hermeticity test, currently missing in mm-size implants.**

I. Introduction

The main aim of bioelectronic medicine is to one day replace conventional chemical drugs with millimeter sized implants. This way, tiny electrical pulses will be locally delivered to a small group of neurons in order to influence and modify biological functions. Developing such implants, however, has brought many new challenges both in the technological and biological domains. One such technical challenge is the packaging of such tiny devices [1]. Conventional active medical implants such as pacemakers have relied on a titanium (Ti) case for packaging the implantable electronics. In recent years, driven by the increased functionality offered by CMOS technologies and the need for further miniaturization, tremendous efforts have been made in designing miniaturized implants and integrating the majority of the components on a single chip [2-3]. Such a single-chip approach, however, would require novel packaging solutions since the Ti case would consume significantly more weight and volume compared to the chip and greatly limit the flexibility of the final implant.

K. Nanbakhsh, W. A. Serdijn and V. Giagka are with the Department of Microelectronics, Faculty of Electrical Engineering, Mathematics and Computer Science, Delft University of Technology, Delft, The Netherlands. (K.Nanbakhsh@tudelft.nl, V.Giagka@tudelft.nl).

V. Giagka is also with the Fraunhofer Institute for Reliability and Micro-integration IZM, Berlin, Germany.

Riina Ritasalo is with Picosun Oy Espoo 02150, Finland.

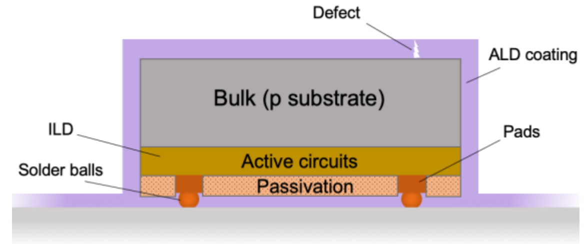

Figure 1. Schematic illustration of a CMOS die coated with an ALD coating layer (dimensions not to scale).

Atomic layer deposition (ALD) is a chemical vapor deposition process that can create a thin (ten to a few hundred nanometers) and conformal coating layer with near hermetic barrier properties [2], [4]. Previous studies have also reported on the biocompatibility and biostability of these layers, making them an attractive packaging solution for mm-sized implants [5]. Such layers, however, could contain micro flaws and defects [6] that could reduce their coating performance and lead to device failure. In conventional Ti packages, the helium leak test is a common method for hermeticity evaluation [7]. This test method, however, is not suitable for mm-sized devices given the lack of cavities within such tiny implants. In the absence of permeable polymers, previously reported humidity sensors are also not applicable [3].

For evaluating the coating performance of ALD layers, DC current leakage and impedance measurements have been reported as sensitive methods for detecting defects in the layer [2], [4], [8]. So far, these measurements have been performed on ALD-coated 2D planar structures and/or on unrepresentative material substrates which will differ from the final device. The barrier properties of thin-coatings, however, are greatly affected by the surface characteristics of the substrate, such as contamination, roughness and aspect ratio [8]. As a result, once the coating has been evaluated and optimized on 2D structures, there is still uncertainty regarding the hermeticity when applied on more complex 3D structures such as an implantable chip. Hence, an evaluation test is still needed for the final device to justify its implantation.

In this study, for the first time, we explore the possibility of using the bulk of the implantable chip as a platform for evaluating the barrier properties of its protective coating. The evaluation method is based on measuring the DC leakage or impedance between the bulk and an exposed platinum (Pt) electrode. This simple approach takes advantage of the conductivity of the bulk and would allow a 3D *in-situ* evaluation of the coating, thus increasing the confidence in its hermeticity prior to implantation. Fig. 1 schematically

illustrates the concept where a bare CMOS chip is coated with a thin ALD layer. The majority volume in such a single-chip implant is occupied by the conductive CMOS bulk, while the metals and active circuits in the chip are protected by the interlayer dielectrics (ILD) and passivation layer. We, therefore, have selected the bulk to be the sensing platform. The advantage of this approach is its simplicity and obviating the need for the design and fabrication of a dedicated sensing platform within the implant.

For this study, test chips have been fabricated in a standard CMOS technology. Section II describes the sample design, the coating process and the experimental set-up used for this work. The measurement results together with a discussion are given in Section III. Finally, the conclusions are drawn in Section IV with a brief description of the future work.

II. Experimental Details

A. Sample

1) CMOS chip

The bulk within standard CMOS processes is typically made of lightly doped silicon. This makes the substrate a low-ohmic layer which will be used in this work as a measurement platform. As a proof of concept, chips were fabricated in a standard 6-metal 0.18 µm CMOS process. For connection to the bulk, a p+ diffusion area of 10 µm×10 µm was used. This creates a low-ohmic contact to the bulk. The chips were glued on a ceramic (alumina) plate and wire-bonded to a metal connection on the plate. For mechanical protection of the wire-bonds and electrical insulation of the metals on the alumina ceramic, polydimethylsiloxane (PDMS) was used. This would enable us to only measure through the bulk and exclude the metal interconnects. PDMS was applied carefully with a dispenser to intentionally leave part of the bulk (bottom and sidewalls) exposed (Fig. 2).

2) ALD coating

Two samples out of four were coated with an alternating ALD multilayer. The samples were first cleaned with isopropyl alcohol and then dried. The thermal ALD process was made using the Picosun R-200 Advanced ALD reactor under reduced pressure (N_2 atmosphere) of about 1 mbar. The ALD is layer-by-layer deposited with N_2-purge in between to separate the different precursors. The deposition started with the growth of the first ALD-material with the needed amount of precursor cycles to reach the required thickness. The same procedure was followed for the second ALD-material. The deposition of the first and second material was repeated 10 times, resulting in a 100 nm ALD-multilayer. More information regarding the ALD multilayer can be found in [2]. Fig. 3 gives a schematic illustration of the ALD coated chips used for this study.

B. Experimental Set-up

All samples (2 non-coated and 2 ALD-coated) were placed in soak within 50 ml vials filled with 1X phosphate buffered saline (PBS) with a composition of 0.0027 M KCl and 0.0137 M NaCl having a pH of 7.4. All experiments were done at room temperature (23 °C). For this work, DC current leakage and electrochemical impedance spectroscopy (EIS) was used to evaluate the barrier properties of the ALD coating. Both measurements were carried out using the

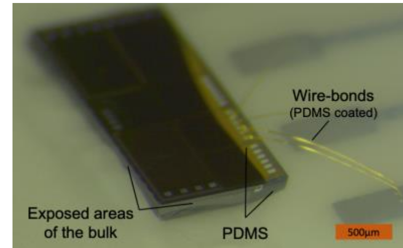

Figure 2. A microscopic image of a chip sample after wire-bonding and PDMS coating.

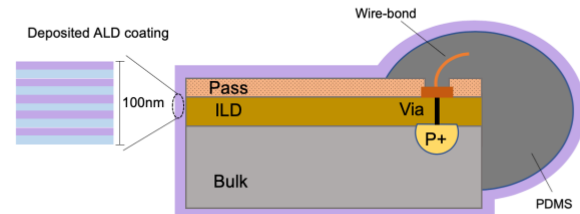

Figure 3. Schematic illustration of the multilayer ALD coating deposited on the sample (dimensions not to scale).

Solartron Modulab where for EIS, the potentiostat in combination with a frequency response analyzer (FRA) was used. In addition, for measuring sub-picoamp current levels, a femtoammeter was connected in series with the module while placing all samples inside a dedicated Faraday cage (more information regarding the measurement module can be found in [9]). All measurements were performed using a two-cell electrode configuration between the CMOS bulk, being the working electrode (WE), and a 2 mm Pt wire, being the counter electrode (CE). Fig. 4 gives a schematic illustration of the soak set-up. DC leakage measurements were carried out by applying a 0.6 V signal between the WE and CE, keeping the WE at ground potential. For EIS, a 10 mV RMS sinusoidal signal in the frequency range of 10 mHz to 100 kHz was used. A low amplitude signal has been chosen to minimize the effects from the measurement signal on the samples. During EIS measurements, the open circuit potential (OCP) between the WE and CE was set to -0.4 V (with the bulk being negative to the Pt). This OCP was measured between the bulk of a non-coated sample and the Pt wire. The OCP for ALD coated samples, however, could not be measured due to the presence of the ALD insulation. Therefore, this potential was used for all EIS measurements.

III. Results and Discussion

A. Measurement Results

Fig. 5 shows the DC measurements results for two ALD coated samples. For comparison, results for one of the non-coated samples is also given in which the current is measured between the bulk and the Pt wire. Results show that for both of the coated samples the leakage currents were <1 pA, while for the non-coated samples the current is four orders of magnitude larger. These results are in agreement with previously evaluated ALD multilayers, confirming their high barrier properties [2]. Impedance measurements were used to characterize and compare the non-coated and coated samples.

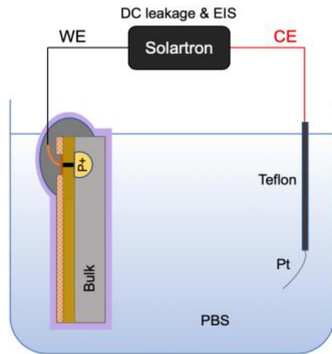

Figure 4. Schematic illustration of the set-up used for DC leakage and EIS measurements.

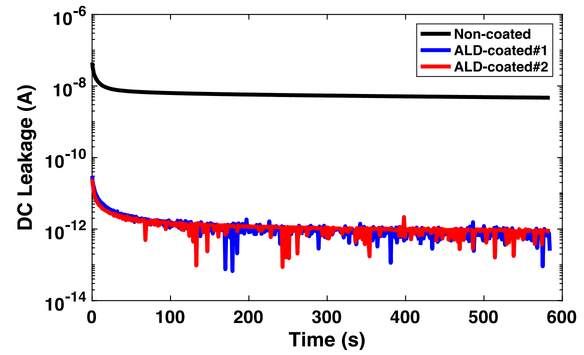

Figure 5. Measured DC current leakage over a duration of 10 min.

Fig. 6 shows the impedance data given as Bode magnitude (|Z|) and phase angle plots over the measured frequency range. For the non-coated sample, a clear constant phase element (CPE) behavior is seen in the middle frequencies (1-100 Hz). The higher frequencies represent the spreading resistance together with the parasitic capacitance present between the connecting WE and CE cables. However, the resistance is more dominant which results in a phase angle around -40°. For the two ALD coated samples, a more capacitive behavior is dominant across the entire measured spectrum. This is the expected behavior when considering the interface to be a parallel plate capacitor with the ALD as the dielectric. The slightly higher impedance magnitude for ALD-coated#2 is mainly due to the manual dispensing of the PDMS, which covered one sample more than the other.

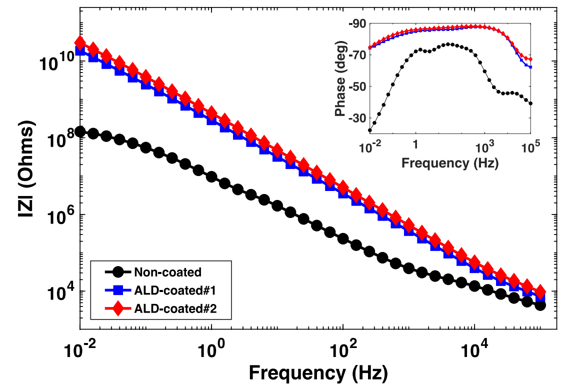

Figure 6. EIS measurements presented as Bode magnitude and phase angle (inset) plots.

To better understand the impedance data, Fig. 7 gives the equivalent circuit model for the non-coated and coated samples. For the exposed bulk (Fig. 7(a)), the silicon creates a thin native oxide layer with a thickness in the range of a few nanometers. As it is seen from the Bode plots, however, this layer is not uniform and thick enough to create a capacitive behavior. Therefore, the exposed bulk to electrolyte interface can be modeled as a CPE in parallel with a resistor representing the polarization resistance (R_F). For the ALD coated sample (Fig. 7(b)), in the absence of any defects, the interface can be represented by a capacitor. Given the higher thickness of the ALD compared the to the native oxide, a lower interface capacitance and therefore, higher impedance is measured for the ALD coated samples. A defect in the layer, however, would expose the silicon bulk to the electrolyte creating a parallel CPE path. Depending on the ratio of these paths, the EIS data will change with the phase angle deviating from an ideal capacitor (-90°) to a more CPE like value (-70° to -80°). The total impedance response of such an interface, therefore, will depend on the aggregate dimensions of these defects and how they will dominate the impedance response at different frequency regimes.

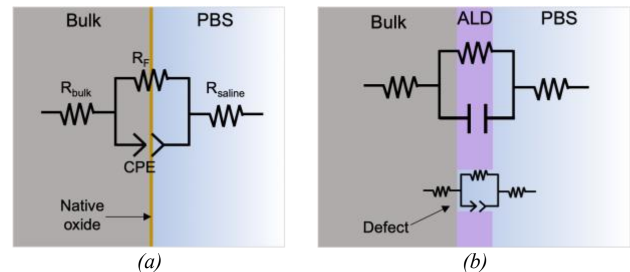

Figure 7. Schematic illustration of the equivalent circuit model for (a) bulk-saline interface, and (b) bulk/ALD-saline interface. (dimensions not to scale).

To investigate how the level of defects could be captured in the impedance results, scratch tests were performed on a coated chip, ALD-coated#2. Scratch testing is a standard technique for adhesion evaluation of thin-film coatings on various substrates [10]. In this work, however, the goal was to intentionally introduce a defect in the ALD layer and observe the change in impedance. Two scratches were made on the edge of the bulk with the second scratch being more aggressive. Measurements were performed in between by placing the sample back in PBS. Scratches were made using a microprobe needle with a 10 µm tip. Fig. 8 shows the impedance magnitude and phase after the first (Scratch #1) and second scratch (Scratch #2). By comparing the results, it can be seen that as more ALD layer is being removed, the impedance results deviate from the initial capacitive behavior and exhibits more an CPE behavior, similar to the non-coated sample. To investigate the reproducibility of the test, a scratch was also created on first coated sample which also resulted in a similar drop in impedance. These results show that EIS measurements with the bulk as the sensing platform, can be used for detecting defects in the ALD layer.

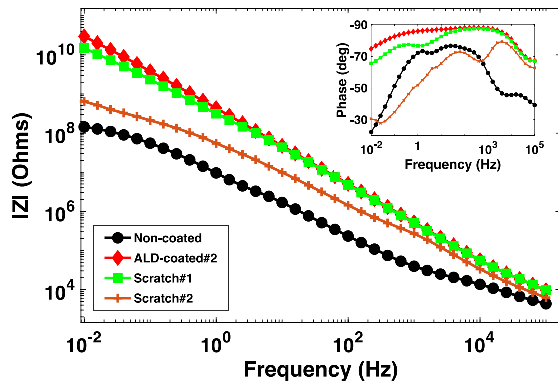

Figure 8. EIS measurement results for an ALD coated sample after first (Scratch#1) and second (Scratch#2) scratch tests on the ALD surface.

B. *Discussion*

Thin-film coatings are a promising packaging solution for bioelectronic medicine. Failure of the coating, however, will result in various chemical and electrochemical reactions that could, in turn, result in performance loss or total device failure [7], [11]. The focus of our group is realizing sensing and monitoring platforms for *in-situ* evaluation of hermeticity for thin-film coated bioelectronic medicine. In [12] we introduced a monitoring platform for tracking water/ion ingress within the different ILD stacks of CMOS chips. Water/ion ingress, however, will only be sensed once penetrated through the top coating, passivation and ILD oxide layer. Evaluation of the outer coating, therefore, would require a different sensing platform which is the focus of this work. Using the bulk, takes advantage of the conductivity of the CMOS substrate and enables a simple *in-situ* evaluation platform for detecting cracks or defects in the outer coating.

The ultimate goal of this work is to have an on-chip measurement unit with the bulk being the sensing platform. This would enable an implant with autonomous *in-situ* hermeticity evaluation. Such an autonomous platform could also be used for long-term hermeticity evaluation during the implant's lifetime. For this reason, we opt for a low-voltage impedance measurement method since the measurement signal is biphasic and no DC current is applied to the exposed electrode. It this study, measurements were carried out between the bulk and a Pt wire. Within the implant, however, it is envisioned that the measurements will be done on chip, between the bulk and a Pt micro-electrode (the electrode intended for stimulation/recording). We do believe that the results reported here are still representative, given that the impedance is dominated by the coated substrate in respect to the exposed Pt wire.

In microelectronic design, the bulk of the chip is usually connected to the ground of the circuit, i.e. the lowest potential. Using the bulk as a sensing platform would, therefore, require novelty in the circuit design. For example, the added circuitry should neither increase the noise nor interfere with the normal operation of the implant. Currently, we are working on the design of such a circuit that could perform the measurements on-chip.

IV. Conclusion & Future Work

In this work, we demonstrate for the first time the feasibility of using the CMOS bulk as a platform for evaluating the hermeticity of thin coating layers on implantable chips. As a proof of concept, off-chip DC leakage and EIS measurements were performed in saline on chips fabricated in a standard CMOS process with and without a deposited coating layer. The coating used in this study was an ALD multilayer with a total thickness of 100 nm. EIS was chosen over DC leakage as a more suitable measurement technique. Future work will focus on designing an on-chip measurement circuit that will enable a fully integrated platform for hermeticity testing.

Acknowledgments

This research was supported by the POSITION-II project funded by the ECSEL JU under grant number Ecsel-783132-Position-II-2017-IA.

References

[1] V. Giagka and W. A. Serdijn, "Realizing flexible bioelectronic medicines for accessing the peripheral nerves – technology considerations," *Bioelectron. Med.*, vol. 4, no. 8, pp. 1–10, 2018.

[2] J. Jeong, F. Laiwalla, J. Lee, R. Ritasalo, M. Pudas, L. Larson, V. Leung, and A. Nurmikko, "Conformal hermetic sealing of wireless microelectronic implantable chiplets by multilayered atomic layer deposition (ALD)," *Advanced Functional Materials*, vol. 29, no. 5, p. 1806440, 2018.V.

[3] P. Yeon et al., "Microfabrication, assembly, and hermetic packaging of mm-sized free-floating neural probes," in Proc. *IEEE Biomed. Circuits Syst. Conf. (BioCAS) 2017*, pp. 608 611. [Online]. Available: https://doi.org/10.1109/BIOCAS.2017.8325214.

[4] C. Li, M. Cauwe, M.; Y. Yang, D. Schaubroeck, L. Mader and M. O. de Beeck, "Ultra-Long-Term Reliable Encapsulation Using an Atomic Layer Deposited HfO2 /Al2O3 /HfO2 Triple-Interlayer for Biomedical Implants," *Coatings,* 2019, 9, 579.

[5] J. C. Souriau, J. M. H. Morales, L. Castagné, G. Simon, K. Amara, B. Boutaud, "Miniaturization and Biocompatible Encapsulation for Implantable Biomedical Silicon Devices," *ECS J. Solid State Sci. Technol. 2015*, 4, P445–P450.

[6] K. Nanbakhsh, R. Ritasalo, W. A. Serdijn, and V. Giagka, "Long-term encapsulation of platinum metallization using a HfO_2 ALD – PDMS bilayer for non-hermetic active implants," *in Proc. IEEE Electron. Comp. Tech. Conf. (ECTC). 2020,* Orlando, FL, USA, May 2020.

[7] A. Vanhoestenberghe and N. Donaldson, "Corrosion of silicon integrated circuits and lifetime predictions in implantable electronic devices,", *J Neural Eng*, vol. 10, p. 031002, 2013.

[8] X. Xie, L. Rieth, R. Caldwell, M. Diwekar, P. Tathireddy, R. Sharma and F. Solzbacher, "Long-term bilayer encapsulation performance of atomic layer deposited Al2O3 and Parylene C for biomedical implantable devices," *IEEE Trans. Biomed. 2013*, Eng. 60 2943–51.

[9] N. Donaldson, C. Lamont, A. Shah Idil, M. Mentink, and T. Perkins, "Apparatus to investigate the insulation impedance and accelerated life-testing of neural interfaces," *J. Neural Eng*, 2018. [Online]. Available: http://iopscience.iop.org/article/10.1088/1741 2552/aadeac.

[10] L. Kilpi, O.M.E. Ylivaara, A. Vaajoki, J. MalmS. Sintonen, M. Tuominen, R.L. Puurunen and H. Ronkainen, "Microscratch testing method for systematic evaluation of the adhesion of atomic layer deposited thin films on silicon," *J. Vac. Sci. Technol. A*, 34 (2016), p. 01A124

[11] K. Nanbakhsh, M. Kluba, B. Pahl, F. Bourgeois, R. Dekker, W. Serdijn, and V. Giagka, "Effect of Signals on the Encapsulation Performance of Parylene Coated Platinum Tracks for Active Medical Implants," in Proc. *41st Int. Conf. of the IEEE Engineering in Medicine and Biology (EMBC) 2019*, Berlin, Germany, Jul. 2019, pp. 3840-3844.

[12] O. C. Akgun, K. Nanbakhsh, V. Giagka, and W. A. Serdijn, "A chip integrity monitor for evaluating long-term encapsulation performance within active flexible implants," in Proc. *IEEE Biomed. Circ. Syst. Conf. (BioCAS) 2019*, Nara, Japan, 17-19 Oct. 2019.