A Charge-Redistribution Phase-Domain ADC Using an IQ-Assisted Binary-Search Algorithm

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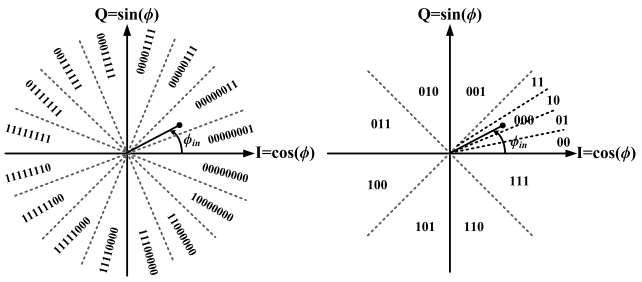
***Abstract*— Phase-domain Analog-to-Digital Converters (Ph-ADCs) have been considered for power-efficient implementation of body-area network transceivers employing phase demodulation. Conventional implementations of the Ph-ADCs, which work based on a full-flash zero-crossing algorithm, use linear resistive/current combiners to determine the thermometer digital code of the signal phase. These architectures suffer from high-accuracy requirements, high-circuit complexity, and high-power consumption. Therefore, in this paper, a new IQ-assisted binary-search algorithm is proposed for implementing the Ph-ADC. The proposed Ph-ADC architecture avoids employing the power-hungry linear combiner. Moreover, for an N-bit Ph-ADC, the proposed algorithm requires only $N+1$ comparisons, whereas the conventional full-flash counterpart demands 2^{N-1} comparisons. Based on the proposed architecture, two different 5-bit charge-redistribution Ph-ADCs are designed and one of them is fabricated in a standard 0.18-μm CMOS technology. The prototype achieves an ENOB of 4.85 bits at 1 MS/s, while dissipating 12.9 μW from a 1.2-V supply.**

***Index Terms*— Phase-domain analog-to-digital converter, IQ-assisted binary search, charge-redistribution Ph-ADC.**

I. Introduction

FREQUENCY-SHIFT keying (FSK) and phase-shift keying (PSK) modulations play important roles in wireless body-area networks and short-range radios [1]–[3]. In wireless receivers, usually, traditional systems extract the amplitude information in the in-phase and quadrature (I/Q) components of the received signal using two matched high-resolution analog-to-digital converters (ADCs), and the signal phase is demodulated in the digital domain. On the other side, the need for driven by low-power wearable and implantable biomedical electronic systems, several architectures have been presented to eliminate the need for high-resolution ADCs in the conventional demodulators by employing phase-domain ADCs (Ph-ADCs) [4]–[11]. It should be noted that the typical resolutions required in such applications are limited to 4 to 6 bits. All of these structures use the full-flash algorithm which originates from detecting zero crossings in rotated versions of the I and Q components of the received signal to determine the signal phase and convert it to digital codes directly, as shown in Fig. 1(a). However, these architectures demand highly linear resistive/current combiners that generate phase shifted sinusoids by combining scaled versions of the I and Q signals, to be discussed in Section II. Therefore, these architectures suffer from high accuracy requirements, high circuit complexity, and high power consumption [10], [12]. Hence, in order to overcome these problems, in this paper, a new IQ-assisted binary-search algorithm, the original idea of which was presented by Liu *et al.* [12], is proposed for implementing the Ph-ADC. The proposed architecture does not demand any linear combiner. Furthermore, compared with conventional full-flash structures which demand 2^{N-1} comparisons for N-bit Ph-ADC, it requires only $N+1$ comparisons. Moreover, the proposed architecture generates the output binary-weighted digital codes directly, without using any thermometer-to-binary decoder.



(a) (b)

Fig. 1. Quantization of the complex-plane (a) by rotated versions of original I and Q axes used in the conventional structures (b) by applying IQ-assisted algorithm used in the proposed structure.

The rest of the paper is organized as follows. In Section II, after reviewing the conventional full-flash algorithm and the previously reported structures for implementing Ph-ADCs, the proposed IQ-assisted binary-search algorithm is introduced. In Section III, based on the proposed algorithm, two different charge-redistribution Ph-ADC architectures are proposed. Section IV presents design considerations of the proposed structures. Section V presents measurement results verifying the efficiency of the proposed Ph-ADC. Finally, the paper is concluded in Section VI.

II. Proposed Conversion Algorithm

The basic idea of IQ-modulation is that an angle modulated sinusoidal signal, which contains the data in its phase (i.e., ϕ_{in}), can be decomposed into two amplitude-modulated sinusoids which are in quadrature, according to

$$cos(2\pi f_c t + \phi_{in}) = cos(2\pi f_c t).I - \sin(2\pi f_c t).Q, \quad (1)$$

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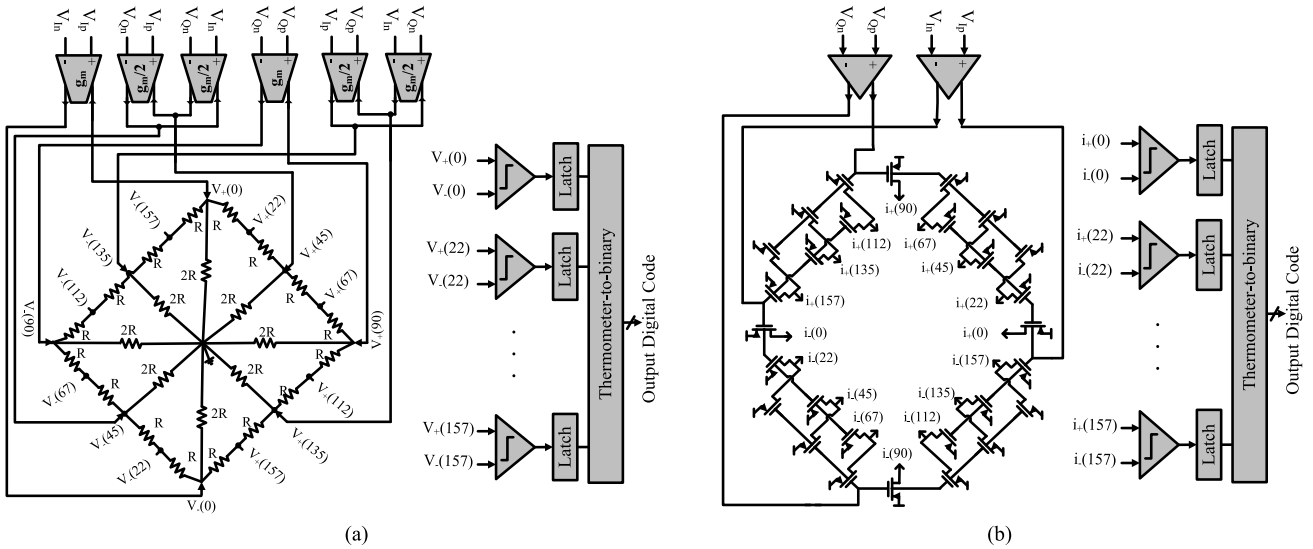

Fig. 2. Schematic of the Ph-ADC implemented based on the full-flash algorithm using (a) resistive combiner [4] and (b) current combiner [10].

where f_c is the carrier frequency, and the signals I and Q representing the amplitudes of the in-phase and the quadrature-phase carriers, respectively, are

$$I = \cos(\phi_{in})$$
$$Q = \sin(\phi_{in}) \tag{2}$$

In the demodulator, one can recombine the two quadrature signals I and Q to extract the input signal phase (i.e., ϕ_{in}). Traditional systems extract the amplitude information in the received I and Q signals using two high-resolution ADCs, and the signal phase is demodulated in the digital domain. In a more efficient way, Ph-ADCs directly extract the digital codes corresponding to the signal phase from the received I and Q input signals. In other words, in order to find the digital code corresponding to the analog signal phase (i.e., ϕ_{in}), the Ph-ADC identifies the quantization interval that contains the signal phase based on either the full-flash algorithm used in the literature [4]–[11] or a new one such as the proposed IQ-assisted binary-search algorithm, to be discussed in the following subsections.

A. Full-Flash Algorithm

In the full-flash algorithm, which is one of the simplest ways to implement the Ph-ADC, the input phase is directly compared with all the transition points between adjacent quantization intervals. It should be noted that instead of comparing the input phase with different levels of the reference phase, it is more convenient to compare the rotated versions of the input phase of ϕ_{in} (i.e., $\phi_{in}+\phi_{LSB}$, $\phi_{in}+2\phi_{LSB}$, $\ldots$, $\phi_{in}+(2^N-1)\phi_{LSB}$) with a reference phase, where ϕ_{LSB} is defined by

$$\phi_{LSB} = \frac{2\pi}{2^N}, \tag{3}$$

and N is the resolution of the Ph-ADC. Since the input signals of the Ph-ADC are I and Q components, it is not possible to access ϕ_{in} directly. Therefore, by using a linear combiner, scaled values of I and Q signals are combined to generate the required rotated versions of ϕ_{in}. After that, in order to determine the output thermometer digital codes, the zero crossings of these rotated versions of I and Q are detected, i.e. [10],

$$-I.sin\frac{m\pi}{2^{N-1}} + Q.cos\frac{m\pi}{2^{N-1}} = 0 \; m = 0, 1, \ldots, 2^{N-1} - 1. \tag{4}$$

In order to generate phase shifted versions of the I and Q components, i.e., the rotated versions of the original I and Q signals, in literature, different linear combiner structures have been reported. One approach is to use a resistive network, as shown in Fig. 2(a) [4]–[9]. This circuit converts the currents of preceding operational transconductance amplifiers (OTAs) to shifted voltages in its different nodes and these voltages are fed into the comparators which act as zero-crossing detectors. The outputs of the comparators form the thermometer digital code corresponding to the input signal phase. Another approach is to use a current combiner that employs trigonometric weighted sizes of transistors as current sources, as shown in Fig. 2(b) [10], [11]. By applying appropriate combination of I and Q input voltages to the gates of the relevant transistors, the current-mode rotated versions of I and Q signals are generated to detect the zero crossings. It is worth noting that the amplitudes of the output voltages of different nodes of the resistive network are not the same, meaning that different slopes in zero crossings can cause nonlinearity in the dynamic behavior of the Ph-ADC, especially in high-resolution converters. Moreover, due to the resistive nature of the structure, in order to have appropriate levels for the comparators' inputs, larger amount of resistors or input currents are required, leading to larger area occupation and larger power consumption, respectively.

B. Proposed IQ-Assisted Binary-Search Algorithm

From the above, it is clear that the circuit architectures implementing the full-flash algorithm not only demand

a highly linear resistive/current combiner, but also suffers from the static power consumption of the required combiner. In order to overcome these problems, a new Ph-ADC architecture that employs an IQ-assisted binary-search algorithm is proposed which not only avoids using a linear combiner, but also requires only $N+1$ comparisons whereas the conventional full-flash counterpart demands 2^{N-1}comparisons. In the proposed algorithm, by using a phase-domain binary search, the reference phase of ϕ_{ref} successively approximates the sampled input phase of ϕ_{in} and in each step, one bit of the output digital code corresponding to the input phase is determined. As the quantization full scale range of the input phase is $[0,2\pi]$, in the first comparison, ϕ_{in} must be compared with $\phi_{ref,1}=\pi$. According to the result, the most significant bit (MSB), i.e., B_1, is determined. Then, in the second comparison, the input phase is compared with $\phi_{ref,2}=\pi/2$ (if $B_1=0$) or $\phi_{ref,2}=3\pi/2$ (if $B_1=1$), and the second bit, i.e., B_2 will be found. This procedure will be repeated until all N bits corresponding to ϕ_{in} are determined or, in other words, the difference between ϕ_{in} and $\phi_{ref,N}$ becomes less than ϕ_{LSB}. It should be noted that the input signals of the converter are the I and Q components defined by (2) and it is not possible to access the input phase (i.e., ϕ_{in}) directly. However, it is obvious that the $\tan(\alpha)$ function relates the I and Q components to the required ϕ_{in} by

$$\frac{Q}{I}=\tan(\phi_{in}). \tag{5}$$

According to (5), instead of comparing ϕ_{in} with different levels of $\phi_{ref,i}$ defined by

$$\phi_{ref,i}=\pi-\sum_{j=1}^{i-1}(-1)^{B_j}\frac{\pi}{2^j}i\geq 2, \tag{6}$$

the ratio of $Q/I=\tan(\phi_{in})$ is compared with $\tan(\phi_{ref,i})$. In other words, a phase-domain binary search algorithm is used to determine the comparison levels of $\phi_{ref,i}$, but these levels are applied to the $\tan(\alpha)$ function block to be comparable with the ratio of the input signals (i.e., Q/I), as shown in Fig. 3. Moreover, since the $\tan(\alpha)$ function presents similar patterns during the quadrants of $[0, \pi/2]$, $[\pi/2, \pi]$, $[\pi/2, \pi]$, and $[3\pi/2, 2\pi]$, the proposed algorithm uses the well-known sub-ranging or two-step method in order to determine the digital code corresponding to the input phase. In other words, the operation of the proposed binary-search algorithm can be divided into two general steps, as shown in Fig. 4. In the first step, the algorithm determines which quadrant of $[0, \pi/2]$, $[\pi/2, \pi]$, $[\pi, 3\pi/2]$ or $[3\pi/2, 2\pi]$ contains the input signal phase (i.e., ϕ_{in}), and consequently the value of the first and the second most significant bits (i.e., B_1 and B_2) will be found. For this purpose, since the value of $\tan(\phi_{ref,1}=\pi)$ is not unique (i.e., $\tan(\pi)=\tan(0)=\tan(2\pi)$), and the levels of $\tan(\phi_{ref,2}=\pi/2)$ or$\tan(\phi_{ref,2}=3\pi/2)$ are also undefined, it is not possible to use the ratio of Q/I to determine B_1 and B_2. Therefore, in order to overcome this problem, determining the signs of I and Q signals, by using two comparisons (i.e., $I=I_p-I_n>0?$, $Q=Q_p-Q_n>0?$) is useful. In other words, determining the sign of Q is equivalent to comparing ϕ_{in} with $\phi_{ref,1}=\pi$, and the comparison of ϕ_{in} with $\phi_{ref,2}=\pi/2$

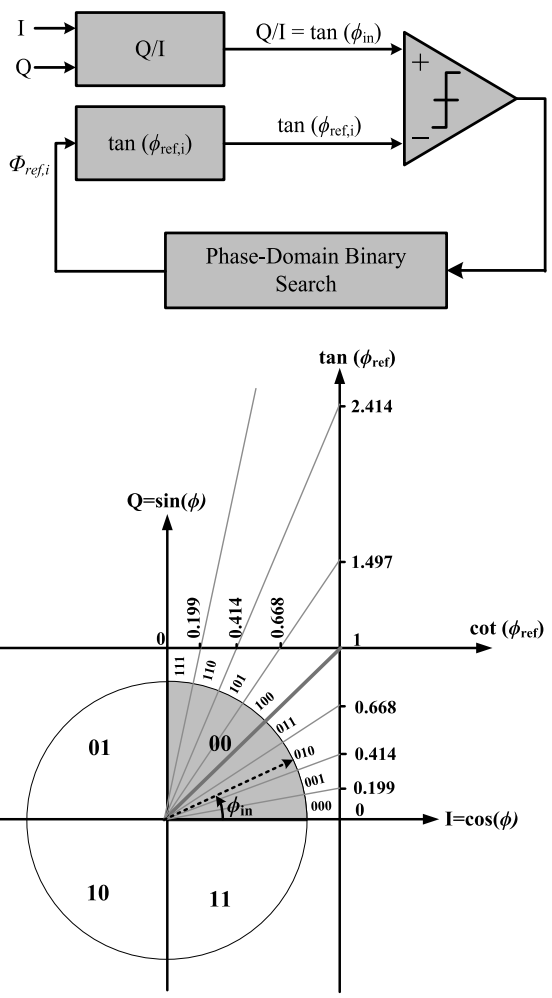

Fig. 3. Principle of the proposed IQ-assisted binary-search algorithm.

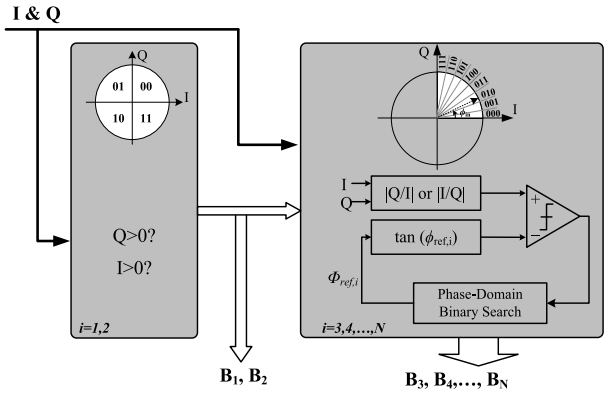

Fig. 4. Principle of the proposed IQ-assisted binary-search algorithm as a two-step ADC.

or $\phi_{ref,2}=3\pi/2$ can be performed by determining the sign of I. After that, in the second step, all these quadrants will be mapped to the first quadrant, and then a binary search is performed only over the range of $[0, \pi/2]$ to determine the remaining $N-2$ digital bits. In order to map the pattern of each quadrant of the IQ-plane to the first quadrant, the absolute value of Q/I (i.e., $|Q/I|$) can be used. However, it should

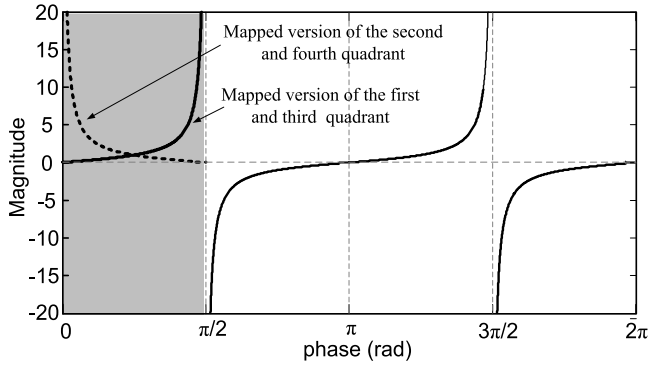

Fig. 5. Graph of the *tan(α)* function.

be noted that although the *tan(α)* graph in the first and third quadrants has the same pattern (meaning that using $|Q/I|$ maps the first and third quadrants to the first one), it has an increasing negative function in the second and the fourth quadrant (meaning that using $|Q/I|$ maps the original pattern to the first quadrant as a decreasing function), as shown in Fig. 5. In order to solve this problem, it is only needed to complement the comparison results corresponding to the *N-2* least significant bits whenever the input phase is located in either the $[\pi/2, \pi]$ or the $[3\pi/2, 2\pi]$ range. After mapping all quadrants to the first quadrant using $|Q/I|$, a binary search is performed only over the range of $[0, \pi/2]$ to determine the remaining *N-2* digital bits. In order to determine the third bit (i.e., B_3)$|Q/I|$ must be compared with $\tan(\pi/4)=1$, meaning that the signal phase of ϕ_{in} is compared with either $\pi/4$ (if $B_1B_2=00$), $3\pi/4$ (if $B_1B_2=01$), $5\pi/4$ (if $B_1B_2=10$), or $7\pi/4$ (if $B_1B_2=11$). For this purpose, the absolute value of I is compared with that of Q (i.e., $|I| > |Q|$?). According to the result of this comparison, B_3 will be found. For determining the fourth bit (i.e., B_4), depending on B_3, the ratio of $|Q/I|$ must be compared with either $\tan(\pi/8)\approx 0.41$ or $\tan(3\pi/8)\approx 2.41$. It is worth noting that for the case that $|Q/I|$ must be compared with $\tan(3\pi/8)$, as illustrated in Fig. 3, it is possible to compare $|I/Q|$ with $\cot(3\pi/8)=\tan(\pi/8)\approx 0.41$ to have simple circuit constrains. This will be discussed in more detail in Section III. In other words, for this purpose $|Q|$ is compared with $0.41|I|$ (if $|I| > |Q|$) or $|I|$ is compared with $0.41|Q|$ (if $|Q| > |I|$). Similarly, for all *N-3* least significant bits, depending on the third comparison, either the ratio of $|Q/I|$ (if $|I| > |Q|$) or $|I/Q|$ (if $|Q| > |I|$) is quantized. The operation of the proposed IQ-assisted binary-search algorithm, for the cases that input phase is in the first or third quadrant of the IQ-plane, is shown in Fig. 6.

In order to compare the proposed IQ-assisted binary-search architecture with the conventional full-flash algorithm, it should be noted that the proposed architecture does not demand any linear combiner. Furthermore, compared with the conventional full-flash structure which demands 2^{N-1} comparisons for *N*-bit Ph-ADC, it requires only *N+1* comparisons. On the other hand, the need for more clock cycles reduces the speed of the proposed algorithm, but this is not a serious issue in applications such as Bluetooth. Moreover, as will be discussed in Section III, the proposed architecture requires track-and-hold (T&H) circuits to charge the capacitors of the employed capacitive array in different bit cycles during the conversion phase which also costs extra power. Therefore, for the intended sampling frequency of several MS/s and lower, the proposed algorithm is superior from a power consumption viewpoint. However, for much higher frequencies (and of course low resolutions), the full-flash structure (excluding the stage preceding the ADC) can be more power efficient.

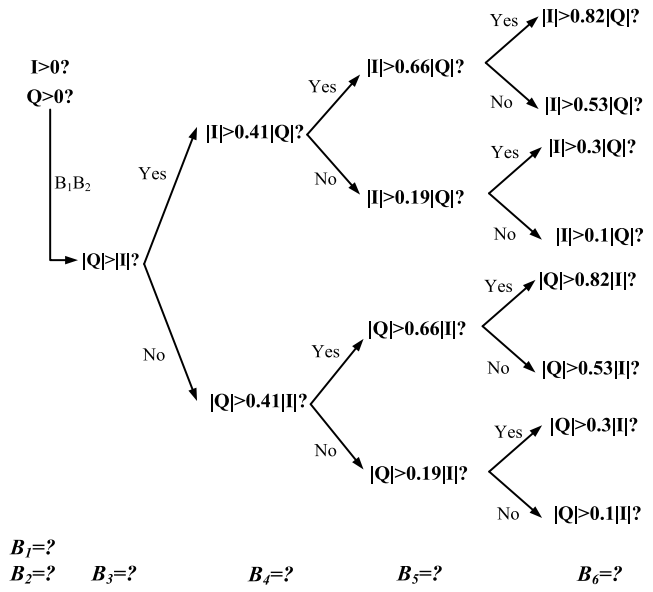

Fig. 6. Proposed IQ-assisted binary-search algorithm for a 6-bit Ph-ADC.

III. Proposed Ph-ADC Circuits

A. Proposed Ph-ADC 1

The schematic of the proposed 5-bit Ph-ADC 1 which works based on the proposed IQ-assisted binary-search algorithm is shown in Fig. 7. The proposed circuit consists of two capacitive digital-to-analog converters (DACs), two track-and-hold (T&H) circuits, four comparators, and a digital control circuit. In this circuit, which works like a two-step ADC, in the first step, the first and the second bits (i.e., B_1, B_2) as well as the third one (i.e., B_3) are determined. Then, in the second step, in order to digitize the ratio of $|Q/I|$ (or $|I/Q|$), the input signals of I and Q are applied to a charge-redistribution ADC, consisting of only one capacitive DAC and one comparator, in such a way that one of them acts as the input signal of the ADC and the other one as the reference voltage of the converter. The operation of the proposed circuit is as follows. In the sampling phase, the input signals of $I=I_p-I_n$ and $Q=Q_p-Q_n$ are sampled and held by the T&H circuits which work as voltage buffers. At the same time, these signals are also sampled on the bottom-plates of the capacitors of the DAC_I and DAC_Q, respectively, while their top plates are connected to the input common-mode voltage V_{cm}. During the first cycle of the conversion phase, the T&H outputs (i.e., I_{Hp}, I_{Hn}, Q_{Hp}, and Q_{Hn}) are applied to the comparators of $Comp_{I1}$ and $Comp_{Q1}$ to determine the signs of the sampled $I_H = I_{Hp}-I_{Hn}$ and $Q_H=Q_{Hp}-Q_{Hn}$ signals. According to

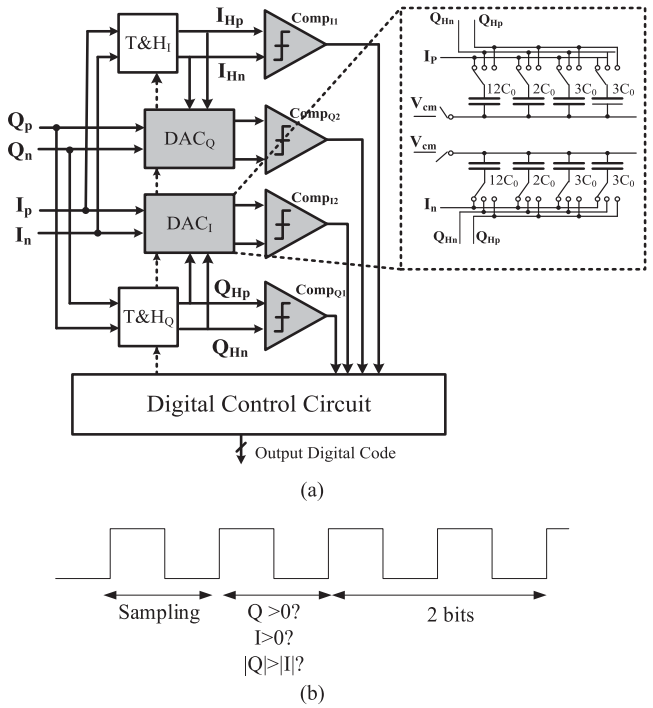

Fig. 7. (a) The schematic and (b) timing diagram of the proposed Ph-ADC 1.

the results, the first and second bits (i.e., B_1 and B_2) will be determined. At the same time, DAC_I and DAC_Q in cooperation with $Comp_{I2}$ and $Comp_{Q2}$ compare the absolute value of I with that of Q (i.e., $|I| > |Q|$?), and the third bit (i.e., B_3) will be also found. For this, the input signal of I must be compared with both Q and $--Q$. In order to perform these comparisons, the upper and lower capacitors of DAC_I are connected to Q_{Hp}, and Q_{Hn}, respectively, and consequently $Comp_{I2}$ compares Q_H with I. Simultaneously, the upper and lower capacitors of DAC_Q are connected to I_{Hn} and I_{Hp}, respectively, and therefore $Comp_{Q2}$ compares -Q with I_H. With the aid of the I and Q signs and these two comparison results, the control logic circuitry determines the value of B_3. In the next clock cycles of the conversion phase, either the ratio of $|I/Q|$ (if $|Q| > |I|$) or $|Q/I|$ (if $|I| > |Q|$) should be quantized. In order to digitize the ratio of I and Qin a binary search algorithm, these signals can be applied to a charge-redistribution ADC if one of them acts as the input signal of the ADC and the other one as the reference voltage of the converter. For this purpose, only one of these four comparators (according to the result of the third comparison, i.e., B_3) and the related DAC and T&H circuit complete the conversion phase to find the remaining digital bits, and the other blocks can be turned off to avoid unnecessary power dissipation. For example, if B_3 determines that $|Q| > |I|$, I acts as the input signal of DAC_I and Q_H is the reference voltage of the charge redistribution ADC. As a result, $T\&H_Q$, DAC_I, and $Comp_{I2}$ perform the remaining cycles of the conversion, and DAC_Q, $T\&H_I$, $Comp_{I1}$, $Comp_{Q1}$, and $Comp_{Q2}$ can be disabled. It should be noted that as the phase is nonlinearly related to the ratio of $|Q/I|$ (or $|I/Q|$), due to the $tan(\alpha)$ and $cot(\alpha)$ relations, in order to extract the linear phase, it is needed to nonlinearly map this ratio onto the quantized phase in the range of [0, $\pi/2$]. In the proposed 5-bit Ph-ADC, functions of $tan(\alpha)$ and $cot(\alpha)$ can be approximated as

$$\begin{aligned}
\tan(\frac{\pi}{16}) = \frac{Q}{I} \approx 0.2 \quad \cot(\frac{7\pi}{16}) = \frac{I}{Q} \approx 0.2 \\
\tan(\frac{2\pi}{16}) = \frac{Q}{I} \approx 0.4 \quad \cot(\frac{6\pi}{16}) = \frac{I}{Q} \approx 0.4 \\
\tan(\frac{3\pi}{16}) = \frac{Q}{I} \approx 0.7 \quad \cot(\frac{5\pi}{16}) = \frac{I}{Q} \approx 0.7 \\
\tan(\frac{4\pi}{16}) = \frac{Q}{I} = 1 \quad \cot(\frac{4\pi}{16}) = \frac{I}{Q} = 1
\end{aligned} \tag{7}$$

According to (7), the approximated values of the $tan(\alpha)$ function determine the comparison levels in $Comp_{Q2}$ corresponding to DAC_Q with Q being the input voltage and I_H being the reference voltage, whereas the $cot(\alpha)$ function determines the comparison levels in $Comp_{I2}$ connected to DAC_I with I being the input voltage and Q_H being the reference voltage. Both DACs have the same differential architecture and each side of the differential network has 20 unit capacitors, which are segmented in such a way that the scaling factors in (7) can be obtained by the differential switching operation. The switching sequence of the capacitive DAC employed in the charge-redistribution ADC is shown in Fig. 8.

B. Proposed Ph-ADC 2

As discussed in the previous subsection, the proposed Ph-ADC 1 determines three MSBs (i.e., B_1, B_2, and B_3) during the first cycle of the conversion phase. Therefore, this structure requires four comparators and two capacitive DACs, leading to an increase in the area occupation and the complexity of the circuit. In order to overcome this problem, a modified structure for Ph-ADC 1 is proposed. This ADC consists of two T&H circuits, one capacitive DAC, one comparator, and a digital circuit, as shown in Fig. 9. The operation of the proposed Ph-ADC 2 is as follows. In the sampling phase, the I and Q voltages are sampled by T&H circuits. In the first clock cycle of the conversion phase, Q_{Hp} and Q_{Hn} are fed into the top plates of the DAC capacitors while their bottom plates are connected to V_{cm}, and the comparator compares $Q_{Hp}$with Q_{Hn}. According to the result, the sign of $Q = Q_{Hp} - Q_{Hn}$, and consequently the first bit (i.e., B_1) are determined. In the second cycle of the conversion phase, similar to the previous cycle, the outputs of the $T\&H_I$ block (i.e., I_{Hp} and I_{Hn}) are connected to the top plates of the capacitors, and the comparator determines the sign of $I = I_{Hp} - I_{Hn}$, and thereby the second bit (i.e., B_2) is found. In the third cycle, the absolute values of I must be compared with that of Q. As the signs of both I and Q signals have been determined during the two previous cycles, only one of the two comparisons mentioned in the proposed Ph-ADC 1 is required to determine the third bit (i.e., B_3). In other words, depending on B_1 and B_2, I is compared with either Q or $-Q$. For this purpose, when the signs of I and Q are the same (or opposite), the bottom plates of the upper and lower capacitors of the DAC are connected to Q_{Hn} (or Q_{Hp}) and Q_{Hp} (or Q_{Hn}), respectively, and

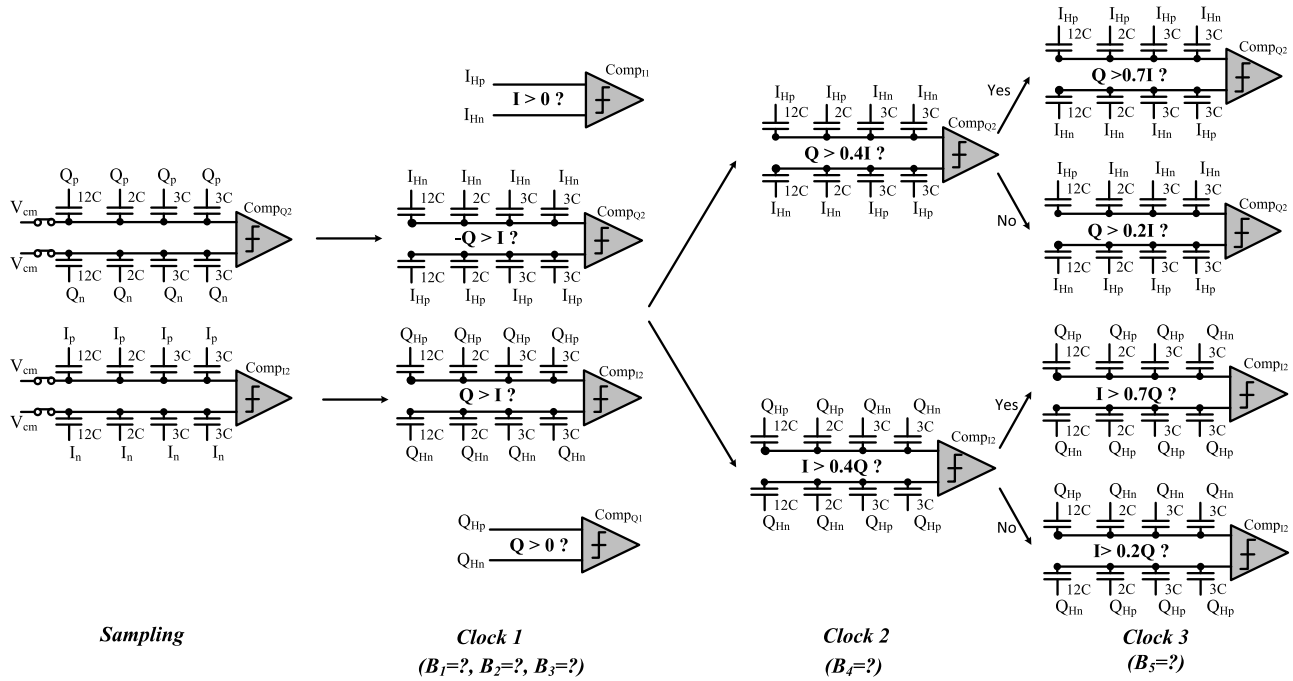

Fig. 8. Switching procedure of the proposed Ph-ADC 1. I and Q signals are assumed to be positive signals (i.e., $I>0$ and $Q>0$).

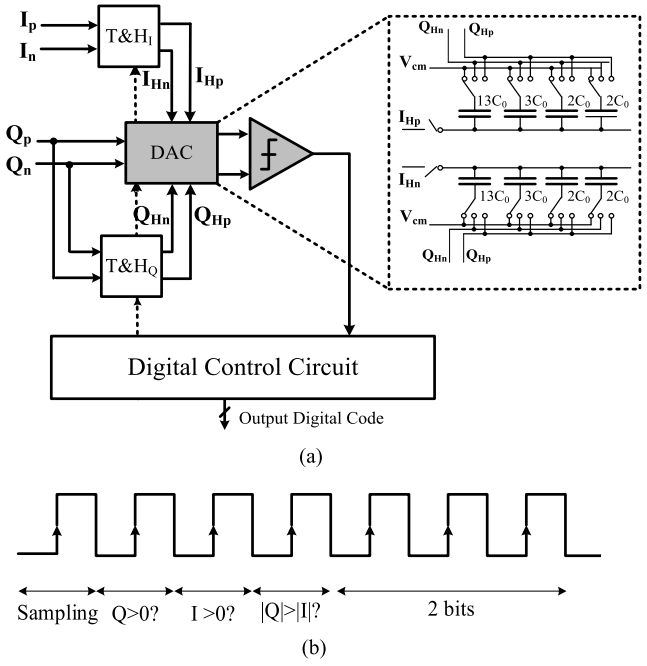

Fig. 9. (a) The schematic and (b) timing diagram of the proposed Ph-ADC 2.

according to the comparison result B_3 will be found. In order to determine the remaining digital bits (i.e., B_4 and B_5), the ratio of $|Q/I|$ or $|I/Q|$, must be digitized using a charge redistribution ADC. Therefore, either I_H or Q_H must act as the input signal of the charge redistribution ADC and the other one as the reference voltage of the converter. Since there is only one capacitive DAC, during the fourth cycle of the conversion, based on the previous comparison, the top plates of the capacitors are connected to I_H (if $|Q| > |I|$) or Q_H (if $|Q| > |I|$), and their bottom plates are connected to Q_H (if $|Q| > |I|$) or I_H (if $|Q| > |I|$), as shown in Fig. 10. After that, during two clock cycles, by using I_H (if $|Q| > |I|$) or Q_H (if $|Q| > |I|$) as the reference voltage of the converter, the ADC will be able to determine the digital bits of B_4 and B_5. It should be noted that if we want to use the same switching sequence as that of the proposed Ph-ADC 1, the capacitor sizes must be modified as shown in Fig. 10.

In order to compare these two proposed circuits, it should be noted that in the proposed Ph-ADC 1, three MSBs are found during the first clock cycle of the conversion phase, but in the proposed Ph-ADC 2, three clock cycles are needed to determine these bits. Moreover, in Ph-ADC 2, an extra clock cycle is needed to feed the input signals to the capacitors before using the charge redistribution ADC. This means that the proposed Ph-ADC 1 is able to work at a higher speed. On the other side, unlike the first structure which demands four comparators and two capacitive DACs, the second circuit requires only one comparator and one capacitive DAC, leading to more area and power saving.

IV. Circuit Design Considerations

A. T&H, Capacitive DAC, and Comparator Blocks

The schematic of the designed T&H circuit is shown in Fig. 11(a) [13] and is used in both proposed architectures. This circuit has favorable energy efficiency and sufficient linearity suitable in this relatively low resolution prototype. During the sampling phase, the input signals are sampled on the sampling capacitors of C_{H1} and C_{H2}. In order to reduce the charge injection of the input switches (i.e., M_8 and M_{10}), two dummy switches (i.e., M_7 and M_9) are used. Then, during the conversion phase, the input samples are buffered by two source followers. Due to the small value of the capacitor network (i.e., using a *2.4 fF* unit capacitor, the total size

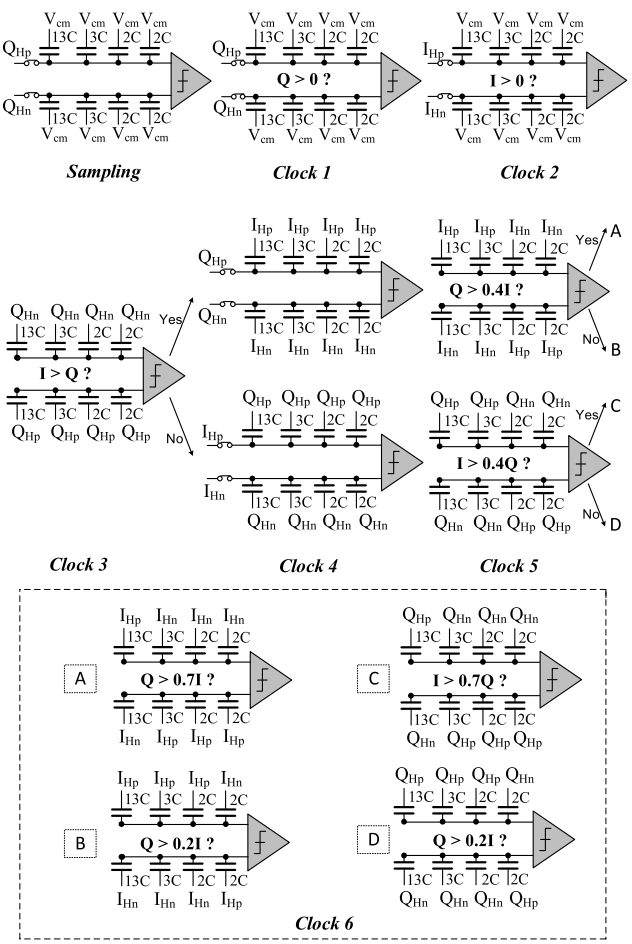

Fig. 10. Switching procedure of the proposed Ph-ADC 2. I and Q signals are assumed to be positive signals (i.e., $I>0$ and $Q>0$).

of the capacitive DAC is around *50 fF* at each input node of the comparator) and the limited driving capability of the T&H circuit, and in order not to be concerned with the kickback noise in the comparator design, the comparator with a static pre-amplifier shown in Fig. 11(b) [14] is adopted. The operation of this comparator, which consists of a preamplifier followed by a dynamic latch, is as follows. When *CLK* is high, the input signal is amplified by the preamplifier and the output nodes V_{op} and V_{on} are precharged. When *CLK* is low, based on the value of the input signals, one output node of the latch goes high and the other goes low. It is worth noting that the precharged nodes of V_{op} and V_{on} may give rise to a static current in the subsequent SR latch during the reset phase if V_{op} and V_{on} are directly connected to the SR latch. For this reason, AND gates are added to isolate the SR latch from the precharged nodes. Both the comparator and T&H circuits have enable signals (i.e., *EN*) thereby saving unnecessary power when these blocks are in the sleep mode.

In order to study the effect of the non-idealities of the T&H circuits, the capacitive DAC, and the comparator on the performance of the proposed Ph-ADC, it should be noted that the linearity of the T&H blocks (i.e., the main limitation of the linearity in the proposed 5-bit Ph-ADC) affects the precision of both the reference voltage and the input sampled signal. In Fig. 11(a), M_3 and M_4 act as current source in

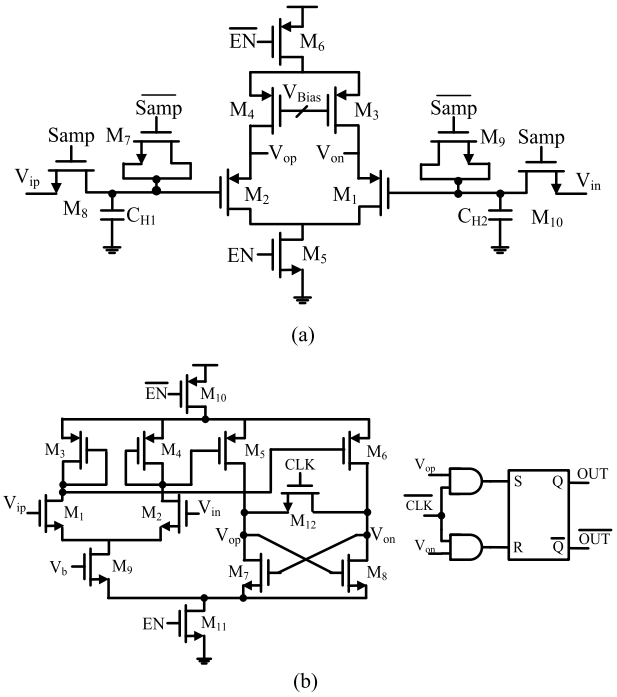

Fig. 11. Schematic of (a) the track-and-hold (T&H) circuit [13] and (b) the comparator circuit [14].

the source-follower structure. Both transient and steady-state non linearities will occur. The steady-state error occurs due to the channel-length modulation of the current sources' devices (i.e., M_3 and M_4) leading to a deviation in the value of $|V_{GS1}|$ and $|V_{GS2}|$ for different values of the input signal being sampled. On the other hand, the main reason for the transient error lies in the incomplete settling of the source-following amplifier which can be reduced when more power is consumed. Another limitation of the linearity in the proposed architecture is the approximation which is applied in determining the comparison levels. It can be shown that in order to generate more accurate comparison levels, the total amount of capacitance of the capacitive DAC has to be increased, leading to an increase in the area and power consumption.

In order to investigate the effect of DAC mismatch on the performance of the proposed structure, a Monte-Carlo simulation of 1000 runs was performed. The values of the unit capacitors (i.e., C) are taken to be independent identically-distributed Gaussian random variables with a standard deviation (i.e., σ/C) of 1%, 5%, and 10%, leading to mean values of 4.9, 4.89, and 4.87 bits for the effective number of bits (ENOB) of the Ph-ADC, respectively. It can be observed that the degradation of the ADC performance due to the capacitor mismatch is negligible. As for the offset voltage of the comparators, the values of the comparator's offsets are taken to be independent identically-distributed Gaussian random variables with a standard deviation of 5mV, 10mV, and 15mV and the results of the Monte-Carlo simulation show that the mean values of the ENOBs are 4.87, 4.8, and 4.74 bits, respectively. It can be observed that similar to the DAC mismatch, the degradation of the ADC performance is again negligible.

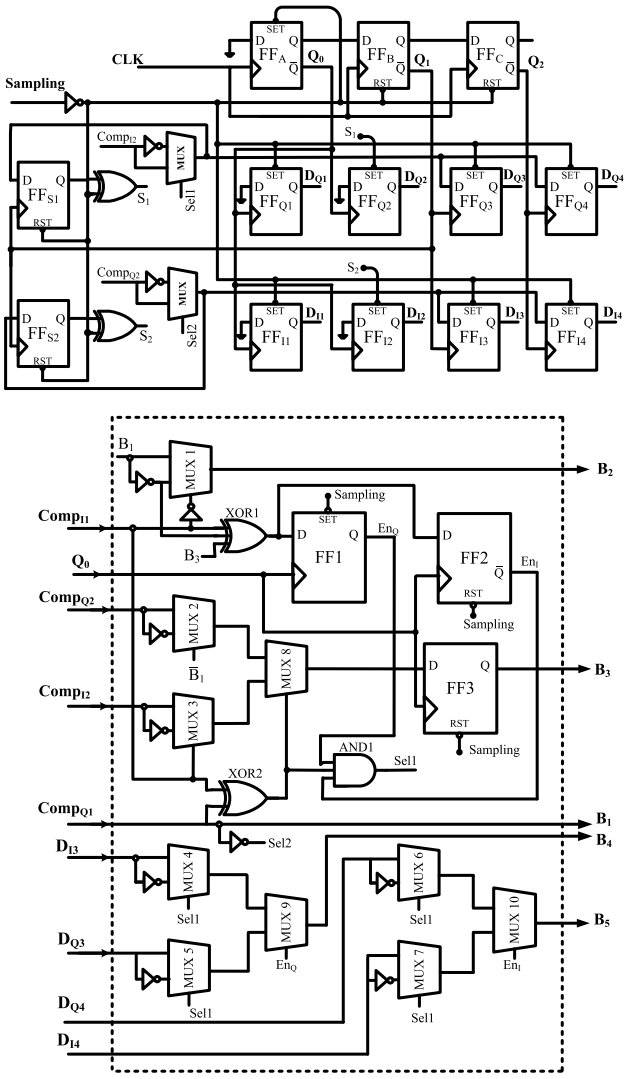

Fig. 12. Schematic of the digital control circuit of the proposed Ph-ADC 1.

B. Digital Control Circuit

The control logic circuit, which is required to implement the proposed Ph-ADCs, consists of two parts. The first part includes control logic that generates the required commands to control the switches in the capacitive DACs and the enable signals. The second part generates the output digital bits (i.e., B_1-B_5) based on the results of the comparisons. In the following, the details of the required digital circuit for implementing the proposed Ph-ADC 1, shown in Fig. 7, are explained. The schematic of the digital control circuit of the proposed Ph-ADC 1 is shown in Fig. 12. In this circuit, the first bit is directly determined based on the comparison which determines the sign of Q and will be saved at the output latch of $Comp_{Q1}$. As for the second bit (i.e., B_2), it will be found based on the sign of I. For more details, if the sign of I which is saved at the output of $Comp_{I1}$, is positive, B_2 has the same value as B_1, and if it is negative, B_2 has the opposite value of B_1. This can be performed through a multiplexer (i.e., *MUX1*) which uses B_1 and $\overline{B_1}$ as inputs and $Comp_{I1}$ as the select signal. Similarly, based on B_1, $Comp_{I1}$, and the results of the two comparisons that compare the absolute values of the input signals, i.e., $Comp_{I2}$ and $Comp_{Q2}$, the value of B_3 will be determined. For this, the digital gates of *MUX2*, *MUX3*, *MUX8*, and *XOR2* are used and the result (i.e., B_3) will be saved in a flip-flop (i.e., *FF3*). In order to find B_4 and B_5, since these bits are determined by the charge redistribution ADC, we have to not only generate the required commands to control the switches of the capacitive DAC, but also extract the output digital bits from the comparison results. As for the required commands for the switches, a *sequencer,* which is basically a shift register, consisting of three flip-flops (i.e., FF_A, FF_B, and FF_C) is used to guess the output bits, and two *code registers* which each consist of four flip flops (i.e., FF_{Q1}-FF_{Q4} and FF_{I1}-FF_{I4}) are used to store the comparison results, and directly control the switches selecting the capacitors of the DACs. It should be noted that, based on the previous comparisons, the code register related to either DAC_I or DAC_Q performs the remaining conversion process. From Fig. 8, it can be observed that during the second clock cycle of the conversion phase, two capacitors of the capacitive DAC are switched. Therefore, the output of the first flip flop in the shift register (i.e., FF_A) controls two flip flops of the code register (i.e., FF_{Q1} and FF_{Q2} or FF_{I1} and FF_{I2}). Furthermore, as the capacitor of *3C* may have to be switched again in the third clock cycle of the conversion phase, the control signal of S_1 will set the related flip flop if revaluing is required in the last clock cycle of the conversion.

Finally, in order to extract the output digital bits B_4 and B_5 from the results of the two comparisons performed during the second and the third clock cycles, the outputs of FF_{Q3}, FF_{I3}, FF_{Q4}, *and* FF_{I4} are applied to *MUX4-MUX7, MUX9*, and *MUX10*. It should be noted that as discussed in Section II, when the input phase is located in the second and the fourth quadrants, the results of the comparisons must be inverted. For this purpose, *MUX4* to *MUX7* are employed.

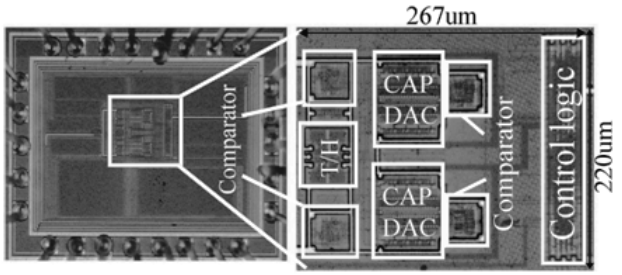

Fig. 13. Die micrograph of the proposed Ph-ADC 1.

V. Measurement Results

In order to verify the efficiency of the proposed architecture, based on the proposed Ph-ADC 1, a 5-bit 1MS/s Ph-ADC has been fabricated in standard 0.18-μm AMS CMOS technology with a 1.2V supply voltage. The unit capacitors of the charge redistribution ADC are implemented as metal-metal capacitors with a small value of *2.4 fF*, which achieves a good trade-off between power efficiency and accuracy. A micrograph of the die is shown in Fig. 13. The active area occupied by the circuit is $267\mu\text{m}\times220\mu\text{m}$.

In order to investigate the static performance of the ADC, Fig. 14 depicts the measured values of the differential

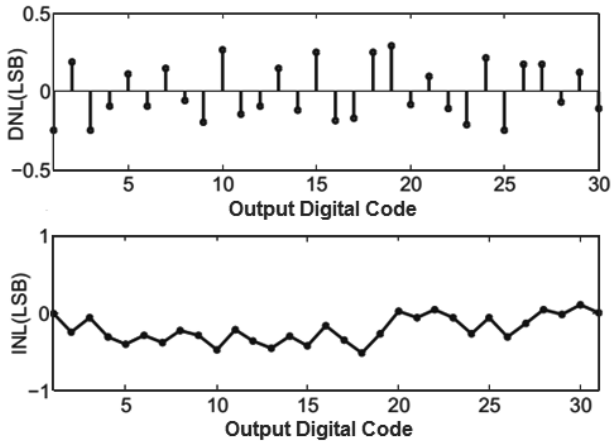

Fig. 14. Measured DNL and INL.

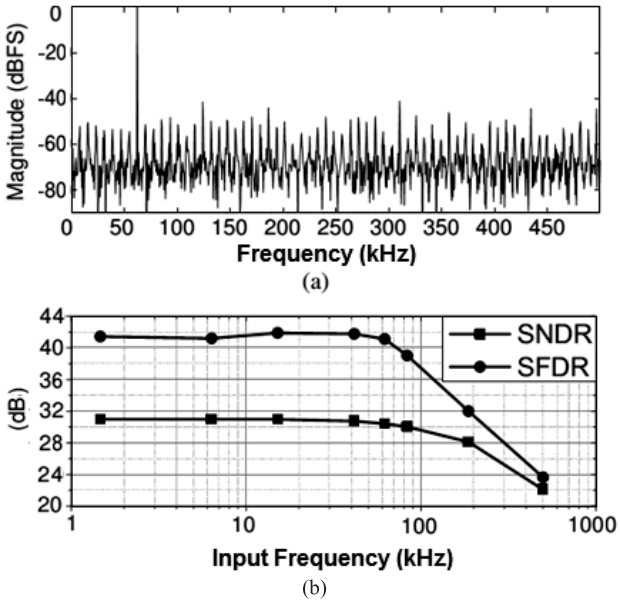

Fig. 15. (a) Measured spectrum (2048-point FFT) at 1 MS/s with a 62 kHz input phase. (b) SNDR and SFDR as a function of input phase frequency.

nonlinearity (DNL) and integral nonlinearity (INL) versus the output digital codes. It can be observed that the maximum values of DNL and INL are 0.29LSB and 0.52LSB, respectively.

As for the dynamic performance of the ADC, it should be noted that the dynamic performance of an amplitude ADC is usually measured with a single-tone input signal. Similarly, a pair of I and Q signals with a single tone phase input, i.e., $\phi_{in}(t) = \pi cos(\omega t)$ is used to characterize the proposed Ph-ADC. Fig. 15(a) illustrates the ADC output spectrum with the input phase close to *62 kHz* at a sampling rate of *1MS/s*. Moreover, the measurement values of the signal-to-noise-and-distortion ratio (SNDR) and the spurious-free dynamic range (SFDR) of the proposed Ph-ADC as a function of the input phase frequency is shown in Fig. 15(b). It can be observed that the SNDR of the proposed Ph-ADC at *62 kHz* is *30.98 dB*, meaning that the effective number of bits (ENOB) of the ADC is *4.85 bits*. The decreased SNDR for increasing input phase frequencies is mainly due to the frequency-dependent nonlinearity of the T&H circuits. In order to study

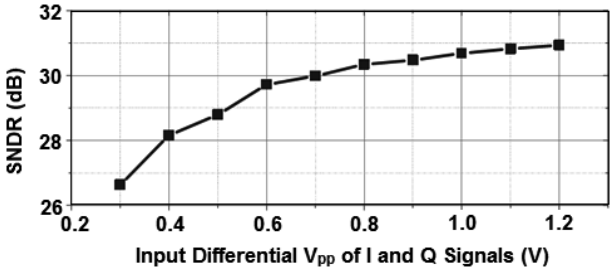

Fig. 16. Measured SNDR as a function of the differential peak-to-peak voltages of the I and Q signals with a phase frequency of 62.01 kHz.

TABLE I
PERFORMANCE COMPARISON OF Ph-ADCs

	[8]	[10]	This work
Technology	0.18 µm	0.13 µm	0.18 µm
Power Supply	1.2 V	1 V	1.2 V
Resolution	4 bits	4 bits	5 bits
Sampling Rate	3.2 MS/s	20 MS/s	1 MS/s
Input Frequency	---	62.5 kHz [a]	62 kHz
Power Consumption	348 µW	25 µW	12.9 µW
ENOB	---	3.61 bits	4.85 bits
Chip Area	0.044 mm^2	0.015 mm^2	0.059 mm^2
FoM_1	---	16.4 pJ/c-s	3.6 pJ/c-s
FoM_2	---	1.34 pJ/c-s	0.13 pJ/c-s

[a] Estimated from [10].

the dynamic range of the proposed ADC, Fig. 16 shows the output SNDR of the Ph-ADC as a function of the differential peak-to-peak voltages of the I and Q signals. The SNDR at *1.2Vpp* is *30.9 dB*, and drops by *3dB* at *0.4 V*, indicating an amplitude dynamic range of *9.5 dB*. As for the power consumption, the proposed ADC consumes *10.76 μA* from a *1.2 V* power supply. The power-consumption contributions of the comparators, the T&H circuits, and the logic circuits are *6.06 μW*, *3.27μW*, and *3.58μW*, respectively.

Finally, in order to compare the efficiency of the proposed Ph-ADC with other works, the well-known Figure-of-Merit (FoM) can be used. The FoM is defined by

$$FoM_1 = \frac{Power}{2^{ENOB} \times 2BW} \tag{8}$$

where BW is the bandwidth of the input signal. It is worth noting that the FoM can also be defined by [15] and [16]

$$FoM_2 = \frac{Power}{2^{2\times ENOB} \times 2BW}. \tag{9}$$

Table I compares the performance of the proposed ADC with other state-of-the-art works using both FoM_1 and FoM_2. It can be observed that the proposed structure presents a competitive performance compared with the other works.

VI. CONCLUSION

In this paper, a new low-power architecture for Ph-ADCs is proposed. The proposed architecture is based on an IQ-assisted binary-search algorithm and not only does not demand any

linear combiner, but also generates the output binary-weighted digital codes directly, without using any thermometer-to-binary decoder. Based on the proposed algorithm, two different 5-bit charge-redistribution Ph-ADCs are designed and one of them is fabricated in a standard 0.18-μm CMOS technology to confirm the efficiency of the proposed architecture.

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