Out-of-Band Immunity to Interference of Single-Ended Baseband Amplifiers Through IM_2 Cancellation

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***Abstract*—The effect of second-order intermodulation (IM_2) distortion produced by out-of-band, high-frequency interference on baseband/IF amplifiers is analyzed using the Volterra series. It is shown that a compensation loop designed to trap nonlinear currents improves the immunity of differential stages to IM_2 distortion generated by local feedback. Measurements of a single-ended amplifier example implementing the proposed method demonstrate an IP_2 increase of more than 30 dB.**

***Index Terms*—Amplifiers, EMI, IM2 cancellation, nonlinear distortion, RFI.**

I. Introduction

ELECTRONIC systems typically use baseband amplification or buffering prior to any A/D conversion and subsequent signal processing. Baseband amplification should preserve signal integrity, without adding any significant noise or distortion. Over time, there has been a tremendous amount of effort to improve in-band noise and linearity performance of amplifier circuits [1], [2]. However, much less attention has been given to the impact of out-of-band interference signals on the operation of a baseband amplifier, and how baseband circuitry can be optimally configured to minimize it [3]. The latter is rapidly gaining importance due to the ever growing number of wireless (RF) aggressors. Some methods have been proposed to address the issue in negative feedback amplifiers on architectural level. These are predominantly based on distortion cancellation by means of symmetry [4] or isolation and subsequent subtraction of error terms [5]–[7]. It is also possible to reduce distortion by modifying the impedance of selected nodes of the amplifier circuit [8]. At the same time, passive filtering approaches at lower frequencies tend to be avoided, in order to reduce cost, board and chip area. In this work, we address the emerging need for low-cost, robust baseband amplifiers, by introducing new design techniques that improve the immunity to out-of-band interference, while not requiring large passive components. To identify the most suitable design approach, we first analyse the imperfections of a traditional negative feedback baseband amplifier, which suffers from undesired down-conversion of out-of-band interferers through second-order intermodulation. After the underlying distortion mechanism is determined, the basis is set for identifying a novel circuit solution that significantly improves the achievable IP_2. In principle, the proposed technique is also applicable to other classes of circuits that suffer from second order intermodulation.

In our analysis, no distinction is made of transistor type or technology (e.g., silicon CMOS/BICMOS or III-V HBT). Furthermore, the proposed IP_2 improvement technique appears to be orthogonal to standard amplifier design methods and does not impact the achievable gain, noise and in-band linearity. Therefore, the IM_2 performance of an amplifier is improved, without affecting the signal transfer quality.

For our investigation, we assume a negative feedback amplifier with a low-pass response that is intended for in-band operation from DC to a corner frequency (f_c) defined by the desired information bandwidth. Out-of-band signals lie at frequencies higher than the upper corner frequency of the information band. Second-order intermodulation is assumed to be the dominant source of interference at baseband. Desensitization and blocking are regarded as high-power effects [9] and are not treated in this work. These are third-order intermodulation mechanisms which are assumed to be of secondary importance to the present analysis. The amplifier under investigation is expected to be functioning well below levels where clipping appears at its output, with distortion products that are comparable to the desired signal (i.e., weak distortion generating mechanisms). A typical interference scenario is illustrated in Fig. 1, where the out-of-band RF signal is represented by tones at frequencies ω_1 and ω_2. The second-order intermodulation product at $\omega_2 - \omega_1$ generated by these tones interacting with the nonlinearity of the baseband negative feedback amplifier falls inside its bandwidth (indicated by a dotted line in Fig. 1).

Designers favor differential circuit topologies when dealing with interference caused by second-order intermodulation (IM_2), because IM_2 distortion products are rejected by a perfectly symmetric differential circuit (i.e., IP_2 approaching

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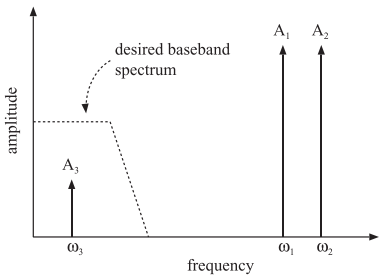

Fig. 1. Out-of-band interferers (ω_1, ω_2) and resulting in-band distortion component at $\omega_3 = \omega_2 - \omega_1$.

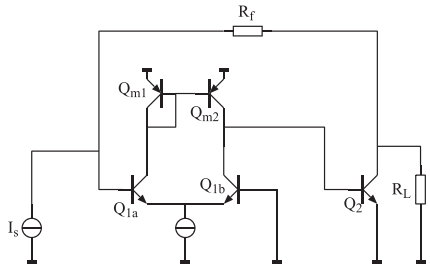

Fig. 2. Circuit of negative feedback amplifier.

infinity) rendering an amplifier insusceptible to EMI. However, a purely differential source and load are required. Also, a differential signal path increases the pin count and packaging costs of the amplifier, and limits the design freedom when interfacing the amplifier to other circuit blocks. Therefore, input and output signals in many applications are single-ended. For example, capacitive sensors are often buffered with a single-ended FET preamplifier to lower their source impedance [10]. To address such practical situations, the emphasis in this work is placed on single-ended input and output configurations, while differential circuits are applied internally. In the following analysis, active components are modelled by a simple equivalent circuit in order to obtain tractable expressions for the Volterra kernels of the system [11]. The transistors are represented by (nonlinear) voltage-controlled current sources [12], where the device transconductance is the foremost source of nonlinearity. In addition, only the linear capacitive component of the transistor input impedance is considered, as this is expected to dominate the frequency response for out-of-band interference [13]. These simplifications are verified by comparing the resulting circuit response with predictions from the full device models in a circuit simulation.

An analysis of the out-of-band distortion mechanism in a typical amplifier circuit is presented in Section II. The dominant distortion error term is identified and a method is suggested to eliminate it. A circuit is proposed in Section III which implements the required cancellation scheme. This is verified through simulations. Section IV outlines a hardware realization of the proposed circuit. Measurement results are presented that show agreement with the theoretical predictions. Finally, a comparison is made of the proposed concept to existing work.

II. Non-Linear Local Feedback in the Differential Stage

The negative feedback (transimpedance) amplifier used for our initial study is shown in Fig. 2. This topology is commonly used as a front-end amplifier in sensor interfaces processing current or charge, often with a (switched) capacitor in the feedback path [14]–[18]. It consists of an input differential stage $Q_{1a} - Q_{1b}$, single-ended output stage Q_2, and feedback resistor R_f. The load impedance is represented by R_L. The biasing of the output stage is not shown and is assumed ideal. An out-of-band signal can couple into the circuit at the input, output, elsewhere along the amplification chain, or via the power supply. The power supply path could easily be eliminated using a filter and is therefore considered trivial. A disturbance appearing at the input is attenuated steadily as it progresses to the output due to the large time constants seen from the internal amplifier poles. The input stage is the most sensitive section of a band limited amplifier to out-of-band interference, because it is subjected to the highest interfering signal level [19]–[21]. In addition, in-band second-order intermodulation distortion generated in response to the interferer by the input stage undergoes full amplification, giving relatively large IM_2 product amplitudes at the output. Therefore, improving the linearity of the input stage should improve interference immunity for the entire amplifier. Of course, this assumes that no in-band attenuation occurs anywhere along the amplification chain, i.e., each amplifier stage implements a signal gain of at least unity. This is distinct from normal operation, where the output stage defines the distortion behavior for in-band signals [22]. The amplitude of an in-band signal is largest at the output of the amplifier, and hence the output stage is assumed to be the greatest source of distortion for in-band signals.

Numerous solutions have been proposed to enhance the immunity of negative feedback amplifiers to EMI. These include the use of a differential pair at the input, or fully differential topologies throughout the amplification chain [4]. However, due to parasitics and imperfections of the active devices, there will always be IP_2 degradation in practice, especially when going from single-ended to balanced configurations (and vice versa). Various methods have been proposed to compensate for second-order distortion effects, such as: the source-buffered differential pair [8], filtered dummy stages [5], [23], the complementary differential pair [6], the double differential pair [7], and frequency-dependent local feedback [24]. While the emphasis in these studies is invariably placed on ensuring that the differential output is free from down-converted distortion, the effect of the distortion on the input of the stage is often overlooked. In this work, it will be shown that local feedback of nonlinear products in a differential stage is a prime contributor to the overall IM_2 distortion. Thus, a structural improvement in the baseband amplifier's immunity to out-of-band interference must address the design of the differential stage itself.

Volterra series are used to estimate the IM_2/IP_2 generated by the amplifier of Fig. 2 in response to an out-of-band interferer. Since Volterra series analysis can result in expressions with a very large number of terms, especially when feedback is present, a relatively simple model for the active devices in the circuit is employed (outlined in the previous section) as shown

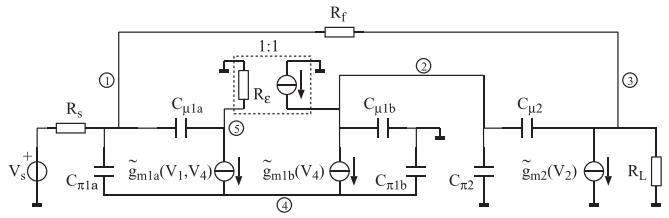

Fig. 3. Equivalent circuit of the negative feedback amplifier.

in the amplifier equivalent circuit of Fig. 3. PNP current mirror $Q_{m1} - Q_{m2}$ is replaced by an ideal current-controlled current source with input impedance R_ϵ. The input current source is approximated by voltage source V_s in series with the large source resistor R_s. Using the admittance matrix $\mathbf{Y}(s)$ of the circuit and its normalized input voltage linear current source vector $\mathbf{IN}_1$ given by

$$\mathbf{IN}_1 = \begin{bmatrix} R_s^{-1} \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix} \tag{1}$$

the linear Volterra kernel vector $\mathbf{H}(s_1)$ of the system can be calculated from

$$\mathbf{Y}(s_1) \times \mathbf{H}(s_1) = \mathbf{IN}_1. \tag{2}$$

In order to simplify the resulting expressions, we assume $R_\epsilon \to 0$ and $C_{\mu 2} \to 0$. After computing the first-order Volterra kernel $\mathbf{H}(s_1)$ of the system, we obtain

$$H_{1,1}(s_1) = 2H_{1,4}(s_1) \tag{3}$$

or

$$H_{1,1}(s_1) - H_{1,4}(s_1) = H_{1,4}(s_1). \tag{4}$$

In other words, the steady-state base-emitter voltages of the differential pair transistors are equal but have opposite signs. This is essential for the following analysis and will be referred to again later. The equality of (4) can also be determined directly from inspection of the circuit. From Kirchoff's current law at Node 4, it follows that the current delivered by g_{m1a} and $C_{\pi 1a}$ must flow into g_{m1b} and $C_{\pi 1b}$. For a symmetrical input differential pair: $g_{m1a} = g_{m1b}$ and $C_{\pi 1a} = C_{\pi 1b}$, and all current sourced by g_{m1a} flows into g_{m1b}. All current flowing out of $C_{\pi 1a}$ is sunk by $C_{\pi 1b}$. This condition remains true only if (4) is valid.

To study the interference scenario, a two-tone signal comprising discrete out-of-band frequency components ω_α and ω_β is applied at the amplifier input, such that

$$\omega_\alpha = \omega_\beta + \omega_\gamma \tag{5}$$

where ω_γ represents the (low) in-band radian difference frequency and $s = j\omega$ (i.e., sinusoidal steady state). The second-order intermodulation product at ω_γ that appears at the output of the amplifier due to the interaction between ω_α and ω_β is given by $H_{2,3}(s_\alpha, -s_\beta)$. It is obtained from the second-order Volterra kernel $\mathbf{H}(s_1, s_2)$, which is calculated using

$$\mathbf{Y}(s_1 + s_2) \times \mathbf{H}(s_1, s_2) = \mathbf{IN}_2 \tag{6}$$

where $\mathbf{IN}_2$ is the second-order nonlinear current source vector

$$\mathbf{IN}_2 = \begin{bmatrix} 0 \\ -I_{NL2,g_{m1b}}(s_1, s_2) \\ -I_{NL2,g_{m2}}(s_1, s_2) \\ I_{NL2,g_{m1a}}(s_1, s_2) + I_{NL2,g_{m1b}}(s_1, s_2) \\ -I_{NL2,g_{m1a}}(s_1, s_2) \end{bmatrix}. \tag{7}$$

Individual nonlinear current contributions are given by [11]

$$I_{NL2,g_{m1a}}(s_1, s_2) = \frac{I_{C1a}}{2V_t^2}\left(H_{1,1}(s_1) - H_{1,4}(s_1)\right) \times \left(H_{1,1}(s_2) - H_{1,4}(s_2)\right) \tag{8}$$

$$I_{NL2,g_{m1b}}(s_1, s_2) = \frac{I_{C1b}}{2V_t^2} H_{1,4}(s_1) H_{1,4}(s_2) \tag{9}$$

$$I_{NL2,g_{m2}}(s_1, s_2) = \frac{I_{C2}}{2V_t^2} H_{1,2}(s_1) H_{1,2}(s_2). \tag{10}$$

If the transistors of the differential pair are biased identically so that $I_{C1a} = I_{C1b} = I_{C1}$, then it follows from (4) that:

$$I_{NL2,g_{m1a}}(s_1, s_2) = I_{NL2,g_{m1b}}(s_1, s_2) = I_{NL2,g_{m1}}(s_1, s_2) \tag{11}$$

with

$$I_{NL2,g_{m1}}(s_1, s_2) = \frac{I_{C1}}{2V_t^2} H_{1,4}(s_1) H_{1,4}(s_2). \tag{12}$$

Equation (6) must be solved in order to calculate $H_{2,3}(s_\alpha, -s_\beta)$

$$\mathbf{H}(s_1, s_2) = \mathbf{Y}^{-1}(s_1 + s_2) \times \mathbf{IN}_2. \tag{13}$$

Note, that $\mathbf{IN}_2$ can be represented as a linear combination of the nonlinear current sources of each amplifier stage

$$\mathbf{IN}_2 = \mathbf{IN}_{2,g_{m1}} + \mathbf{IN}_{2,g_{m2}} \tag{14}$$

where, from (7) and (11)

$$\mathbf{IN}_{2,g_{m1}} = \begin{bmatrix} 0 \\ -I_{NL2,g_{m1}}(s_1, s_2) \\ 0 \\ 2I_{NL2,g_{m1}}(s_1, s_2) \\ -I_{NL2,g_{m1}}(s_1, s_2) \end{bmatrix} \tag{15}$$

$$\mathbf{IN}_{2,g_{m2}} = \begin{bmatrix} 0 \\ 0 \\ -I_{NL2,g_{m2}}(s_1, s_2) \\ 0 \\ 0 \end{bmatrix}. \tag{16}$$

From (13) and (14)

$$\mathbf{H}(s_1, s_2) = \mathbf{Y}^{-1}(s_1 + s_2) \times \mathbf{IN}_{2,g_{m1}} + \mathbf{Y}^{-1}(s_1 + s_2) \times \mathbf{IN}_{2,g_{m2}}. \tag{17}$$

$\mathbf{H}(s_\alpha, -s_\beta)$ can now be obtained by substituting ω_α and ω_β into (17). The first stage is expected to yield the dominant

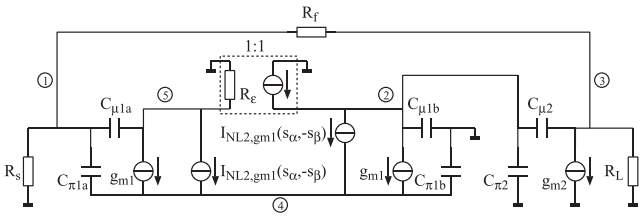

Fig. 4. Input stage nonlinear source equivalent circuit.

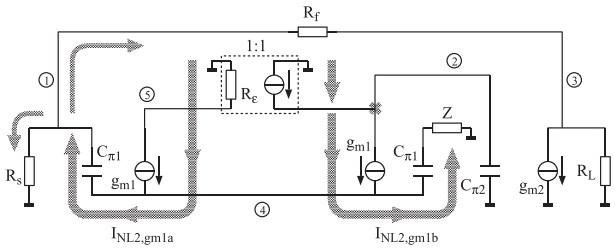

Fig. 5. Fully symmetrical nonlinear current distribution.

nonlinearity, since both ω_α and ω_β are out-of-band due to the low-pass characteristic of the amplification chain. We, therefore, concentrate on the first term of (17)

$$\mathbf{H}(s_\alpha, -s_\beta) \approx \mathbf{Y}^{-1}(s_\gamma) \times \mathbf{IN}_{2,g_{m1}}. \tag{18}$$

$I_{NL2,g_{m1}}(s_\alpha, -s_\beta)$ is the nonlinear current component of each of the differential pair transistors (11). Evaluating this equation to find $H_{2,3}(s_\alpha, -s_\beta)$ is equivalent to determining how $I_{NL2,g_{m1}}$ contributes to the second-order intermodulation voltage V_3 at Node 3 in the equivalent circuit of Fig. 4. Dependent sources g_{m1} and g_{m2} in Fig. 4 are the respective linear transconductances associated with the collector currents of Q_1 and Q_2 in Fig. 2. Two mechanisms through which the sources $I_{NL2,g_{m1}}(s_\alpha, -s_\beta)$ affect the output node can be identified:

- *Mechanism 1*: Direct feed-through via nodes 2 and 5, i.e., from the output of the differential pair, to the output of the amplifier.
- *Mechanism 2*: Feedback of the second-order intermodulation voltage from Node 4 to Node 1. From Node 1 this signal passes directly through the feedback network to the output, or it reaches the output after being re-processed by the amplification chain.

It can immediately be seen from Fig. 4 that for R_ϵ approaching zero, the current mirror delivers the same signal to Node 2 that is subtracted by $I_{NL2,g_{m1}}(s_\alpha, -s_\beta)$ (i.e., *Mechanism 1*). As a result, no IM_2 voltage swing appears at Node 2. This compensation is absent from Node 4, where both nonlinear currents are injected (i.e., *Mechanism 2*). The injected current divides between $C_{\pi 1a}$ and $C_{\pi 1b}$, and appears at the outputs of the devices through their transconductances. This nonlinear, local feedback can disturb the symmetry of the differential pair and thereby allows a common-mode signal to propagate to the output of the amplifier. According to (4), the input signal divides exactly between the two transistors in the differential stage. Furthermore, since ideal transconductors are used in the model and the current mirror is also ideal, a purely differential-mode signal is sourced by the output of the stage. Therefore, the interferer drives and loads the differential stage with perfect symmetry. Despite that, its second-order products are not handled symmetrically, and a fraction of the nonlinear distortion appears at the output of the circuit.

A. Discussion

Under certain conditions, complete cancellation of the nonlinear currents $I_{NL2,g_{m1}}(s_\alpha, -s_\beta)$ occurs at Node 2 in Fig. 4. For example, their combined contribution to V_3 can be brought to zero if these currents divide between $C_{\pi 1a}$ and $C_{\pi 1b}$ after being injected into Node 4. Current division is achieved by replacing the short circuit at the (grounded) inverting input of the differential stage by an impedance (Z) of the appropriate value. Alternatively, it can be shown that for a particular I_{C1}—which is the collector bias current of each of the equally biased differential stage transistors—the components of $I_{NL2,g_{m1}}(s_\alpha, -s_\beta)$ are distributed along the amplification chain in such a way that their contributions at the output node sum to zero. Such solutions will work for a particular frequency set $\omega_\alpha, \omega_\beta$, introduce additional noise due to the real part of Z, or fix the bias and limit the design freedom for the first stage.

It is interesting to note that dividing the nonlinear currents $I_{NL2,g_{m1}}(s_\alpha, -s_\beta)$ equally between $C_{\pi 1a}$ and $C_{\pi 1b}$, where $I_{NL2,g_{m1a}}(s_\alpha, -s_\beta) = I_{NL2,g_{m1b}}(s_\alpha, -s_\beta)$ (i.e., retaining the symmetry of the differential pair) does not result in complete cancellation of the nonlinear current components at the output of the amplifier in general. This is illustrated with the aid of the schematic shown in Fig. 5. The nonlinear current flow due to each transistor of the input differential pair is annotated. The 1:1 current mirror load ensures that perfect compensation occurs at Node 2. However, a portion of the current $I_{NL2,g_{m1}}(s_\alpha, -s_\beta)$ injected into Node 1 is still able to reach the load via feedback resistor R_f. This is true for a single component implementation of Z, or if a dummy output stage and a symmetrical feedback network are used to realize impedance Z across a broader bandwidth. In both cases, it is possible to develop a differential signal between two internal nodes that is free of second-order intermodulation. However, we are interested in developing a single-ended output without passive baluns (e.g., avoiding use of a transformer balun to convert an internal, differential signal to a single-ended output).

III. Novel Method for Nonlinear Feedback Compensation

A new method to reduce the undesired local feedback of even-order distortion components and IP_2 limitations in baseband amplifiers with single-ended input/output is proposed in this section. The principle is illustrated in Fig. 6. Unity-gain current mirrors $G_{1..4}$ copy all of the current components (linear and nonlinear) at the outputs of the differential stage. Mirrors G_1 and G_2 pass the difference between the output currents on to the second stage. The nonlinear currents are identical and common to both outputs, as indicated by arrows in Fig. 6. Their difference is zero, which prevents these currents $I_{NL2,g_{m1a}}(s_1, s_2) = I_{NL2,g_{m1b}}(s_1, s_2)$ (11) from reaching the

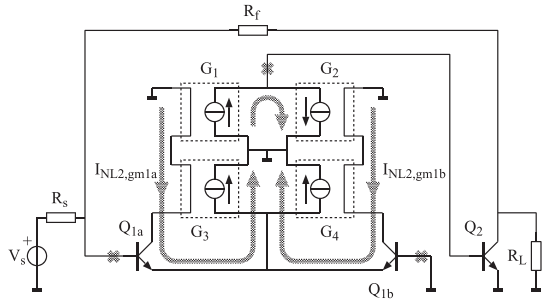

Fig. 6. Proposed nonlinear local feedback compensation topology.

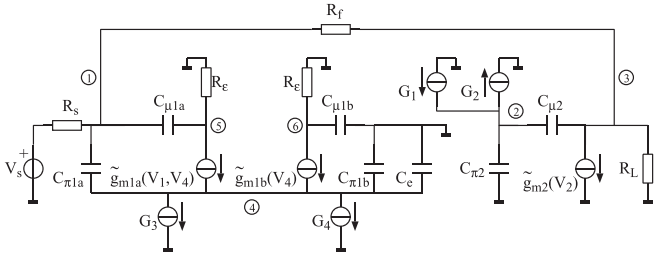

Fig. 7. Equivalent circuit of the proposed amplifier with IM_2 compensation.

base of Q_2. The function of G_1 and G_2 is therefore analogous to the current mirror in Fig. 2, and addresses *Mechanism 1* as outlined in the previous section. Additionally, G_3 and G_4 subtract the sum of the nonlinear currents from the common node of Q_{1a} and Q_{1b} in the proposed circuit, thereby preventing any even-order voltages from developing at this node. This eliminates local feedback to the input through *Mechanism 2* (also outlined in the previous section). In the example of Fig. 6, the nonlinear currents are sensed at the collectors of the differential pair transistors Q_{1a} and Q_{1b} and then pulled from their emitters by G_3 and G_4. Conceptually, it is possible to combine both sensing and feeding at the emitters of Q_{1a} and Q_{1b} by grounding the emitters. This results in a push-pull pair [25]. However, the amplifier inputs would then have to be driven differentially which is not possible in this case (i.e., a single-ended input is assumed).

The amplifier of Fig. 6 is analyzed in greater detail by considering its simplified nonlinear equivalent circuit shown in Fig. 7. Currents sourced by G_1 to G_4 model the outputs of the unity-gain current mirrors, and resistors R_ϵ model the (arbitrarily low) mirror input resistance. Practical circuit parameter values corresponding to commercially available discrete bipolar devices are assumed. The differential pair transistors are biased identically, so $g_{m1a} = g_{m1b} = g_{m1}$,$C_{\pi 1a} = C_{\pi 1b} = C_{\pi 1}$ and $C_{\mu 1a} = C_{\mu 1b} = C_{\mu 1}$. The first-order Volterra kernel of the system is calculated using (1) and (2). From this can be shown that

$$\lim_{R_\epsilon \to 0} \frac{H_{1,1}(s_1)}{H_{1,4}(s_1)} = \frac{C_{\pi 1a} + C_{\pi 1b}}{C_{\pi 1a} + C_{\mu 1a}}. \tag{19}$$

As stated in the previous section, the condition of (4) is essential for second-order distortion minimization, and from (19) it follows that:

$$C_{\pi 1b} = C_{\pi 1a} + 2C_{\mu 1a}. \tag{20}$$

Since Q_{1a} and Q_{1b} are expected to have the same operating point (i.e., $C_{\pi 1b} = C_{\pi 1a}$) in an actual implementation, (20) is not satisfied unless an external capacitor C_e of value $2C_{\mu 1a}$ is added between Node 4 and ground in the circuit of Fig. 7 (i.e., connected in parallel with $C_{\pi 1b}$).

We proceed with the analysis under the assumption that (20) holds, while all other parameters of the input differential pair transistors remain identical. The second-order Volterra kernel is then determined as outlined in (6)–(13). The second-order, nonlinear current source vector $\mathbf{IN}_2$ is given by

$$\mathbf{IN}_2 = \begin{bmatrix} 0 \\ 0 \\ -I_{NL2,g_{m2}}(s_1, s_2) \\ 2I_{NL2,g_{m1}}(s_1, s_2) \\ -I_{NL2,g_{m1}}(s_1, s_2) \\ -I_{NL2,g_{m1}}(s_1, s_2) \end{bmatrix}. \tag{21}$$

Taking $I_{NL2,g_{m1}}(s_1, s_2)$ and $I_{NL2,g_{m2}}(s_1, s_2)$ as parameters, (13) is solved in order to determine $H_{2,3}(s_\alpha, -s_\beta)$. If it is assumed that R_ϵ and $C_{\mu 2}$ approach zero, this is given by (22). A similar result is obtained for a finite $C_{\mu 2}$, except that the expression becomes significantly more involved. Note that (22), as shown at the bottom of the page is independent of $I_{NL2,g_{m1}}(s_1, s_2)$, implying that the input stage nonlinear IM_2 current is completely cancelled at the output node (22), shown at the bottom of the page. Thus, if $\mathbf{IN}_2$ is once more considered as a linear combination of the distinct contributions of the first and second amplifier stages (14), evaluating (17) will result in zero as the first term of the equation. This suggests that the first stage is fully compensated and that any even-order intermodulation at the output arises from the output stage nonlinearity.

The $H_{2,3}(s_\alpha, -s_\beta)$ computed for the amplifier of Fig. 7 is compared to $H_{2,3}(s_\alpha, -s_\beta)$ for the reference circuit of Fig. 3. The results are plotted in Fig. 8 for ω_β swept from 1 MHz to 10 GHz, while ω_γ is kept constant at 1 kHz. The simple transistor model is used initially both for Volterra series analysis and simulations. This is later substituted by a full transistor model

$$H_{2,3}(s_\alpha, -s_\beta) = \frac{s_\gamma C_{\pi 2}\left[s_\gamma\left(C_{\pi 1} + 2C_{\mu 1}\right) + 2g_f + 2g_s\right]}{s_\gamma^3 2g_{m1}g_{m2}g_f\left(2C_{\mu 1}C_{\pi 2}g_L + C_{\pi 2}C_{\pi 1}g_L + 2C_{\pi 2}C_{\mu 1}g_f + C_{\pi 2}C_{\pi 1}g_f\right)} \cdot \frac{I_{NL2,g_{m2}}(s_\alpha, -s_\beta)}{\left(2C_{\pi 2}g_L g_f + 2C_{\pi 2}g_s g_L - 2C_{\mu 1}g_{m2}g_f + 2C_{\pi 2}g_s g_f\right)} \tag{22}$$

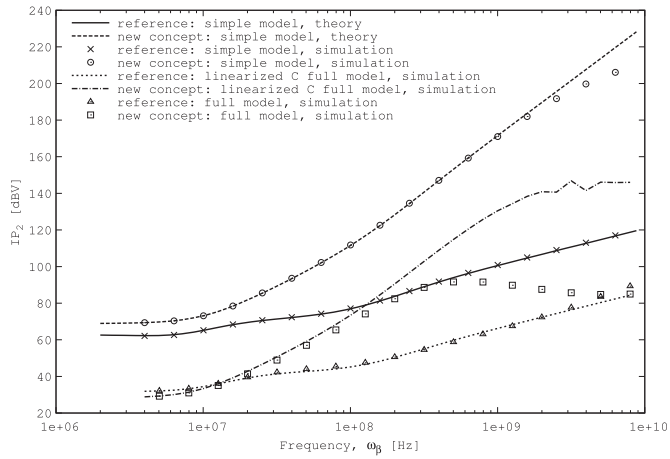

Fig. 8. IP_2 for the circuits of Fig. 3 (i.e., the reference circuit) and Fig. 7.

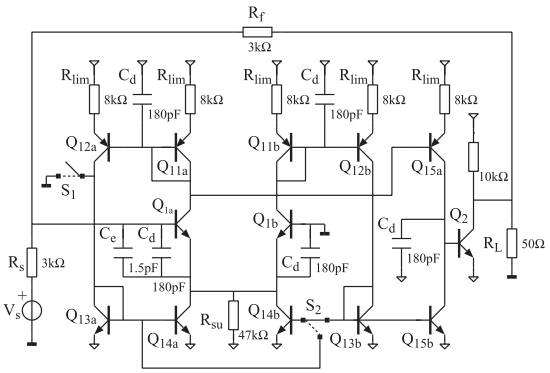

Fig. 9. Practical transistor circuit for the proposed concept of Fig. 6.

with linearized C_π and C_μ, obtained by setting the C_{je}, C_{jc}, and T_f parameters of the SPICE model to zero, and replacing C_{je} and C_{jc} by linear capacitances of the appropriate value. The Volterra series analysis becomes prohibitively complex at this stage, so the circuit response is computed from SPICE simulations only. Finally, full transistor models as supplied by the manufacturer are used in simulation. Circuit biasing is implemented with ideal sources. From the curves calculated from the Volterra-series and simulated using SPICE plotted in Fig. 8, it can be seen that the proposed topology yields a considerably higher IP_2, especially for higher values of ω_β. Note, that there is an offset between the simple transistor model and the linearized-C full model due to device parasitics that are unaccounted for. Nevertheless, both models follow the same trend, thus verifying the concept. From simulation results using the full transistor model, it appears that the impact of nonlinear capacitances is considerable, especially at higher frequencies. They degrade the nonlinear local feedback compensation somewhat, but a superior IP_2 is still realized.

IV. Design Example

To further validate the proposed concept, a practical amplifier circuit is built and measured. Its topology is shown in Fig. 9. In this configuration, transistors $Q_{11} - Q_{14}$ form a positive feedback loop that is stable across a wide range of signal levels. To regulate the bias of the input differential pair, current limiting resistors $R_{\rm lim}$ are used as degeneration at the emitters of Q_{11} and Q_{12}. These resistors also increase the output impedance of each PNP current source. To ensure that the circuit does not remain in an undefined state at power-up, a start-up resistor $R_{\rm su}$ is connected between the common node of Q_{14a}, Q_{14b}, and ground. The resistor value is large enough so that it does not disturb the circuit bias point under normal operation. The external balancing capacitor C_e is added to satisfy the condition of (4) for maximizing IP_2 at the output. This is placed on the opposite transistor of the differential stage than initially surmised by (20) and shown in Fig. 7, because of the output capacitance of the tail current source $Q_{14a} - Q_{14b}$. This parasitic capacitance effectively adds to the balancing capacitor and overcompensates the circuit, necessitating a corresponding reduction of the latter. In this case, the parasitic capacitance is larger than C_e, so a negative capacitor is needed, which is equivalent to a positive C_e on the opposite transistor of the differential stage.

The circuit is implemented with discrete components. As device parameter variation can be significant when working with discretes, matched transistor arrays are used. Inersil's HFA3046/3127 (5 x NPN, $f_t = 8$ GHz, $\beta = 130$ at $I_c = 10$ mA) and HFA3128 (5 x PNP, $f_t = 5.5$ GHz, $\beta = 60$ at $I_c = 10$ mA) parts are chosen [26]. These UHF components could result in an amplifier with an out-of-band range in the gigahertz region. To ensure a valid experiment, the bandwidth of the transistors is artificially degraded by placing capacitors (C_d in Fig. 9) across the base-emitter junction of selected transistors. The bandwidth of the amplifier and its out-of-band region is thereby scaled down to a workable level. Three-dimentional electromagnetic analysis with HFSS, suggests that the physical size of a discrete implementation with 0402 size resistors and 0805 size capacitors precludes proper operation of the circuit beyond approximately 100 MHz, due to distributed parameter effects. The capacitors C_d are therefore chosen to achieve an amplifier bandwidth of around 200 kHz and the out-of-band region above 10 MHz. This does not affect the validity of the concept, but ensures that additional design effort is not expended to account for the electrical size of the final implementation.

A reference amplifier is obtained by rearranging selected connections in the circuit of Fig. 9. This is achieved by switching two jumpers on the measurement board (represented by S_1 and S_2 in the schematic). The resulting circuit is equivalent to the basic amplifier of Fig. 2. This approach minimizes the influence of component spread and ensures that both configurations are subjected to exactly the same test signal. The final implementation is shown in Fig. 10.

The amplifiers are measured with a two-tone (ω_α, ω_β) out-of-band signal applied to the input. The difference frequency (ω_γ) is set at 275 Hz so as not to coincide with harmonics of the 50 Hz mains. The second-order intermodulation product detected at ω_γ is measured with a spectrum analyzer connected directly to the output. The output IP_2 calculated for the proposed and reference amplifier designs is plotted in Fig. 11. The results indicate that the proposed circuit exhibits a significantly higher IP_2—more than 30 dB higher—at the onset of the out-of-band region. The improvement diminishes at higher

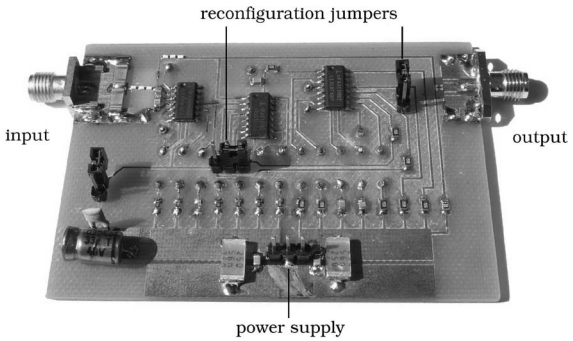

Fig. 10. PCB of the amplifier.

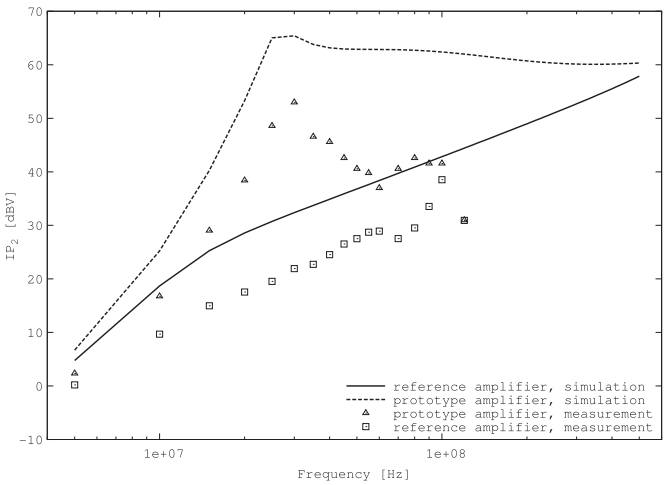

Fig. 11. Simulated and measured output IP_2 for the reference and prototype amplifiers.

frequencies due to secondary nonlinear effects as explained in the preceding section. This drop is sharper than predicted from a lumped component analysis due to the influence of distributed effects above 50 MHz. The latter is in line with the prediction of the 3D EM simulations. There is an approximately equal offset between the measured and simulated IP_2 values for both amplifiers. This appears to be caused by mismatch between passive components and separate transistor arrays, (i.e., two NPN array ICs were needed in the set-up).

The performance of both circuits is also investigated with respect to noise and bandwidth. In Fig. 12 the frequency response of the two amplifiers is shown, together with their input referred noise density. Neither bandwidth nor noise behavior are affected significantly by the activation of the proposed nonlinear, local feedback compensation loop in the prototype. Since both amplifiers have identically configured and biased output stages and implement the same transfer function, their dynamic range is also nearly identical (i.e., approximately 85 dB). It should also be noted that the proposed design method does not place any requirements on the biasing of the differential stage. Noise optimization can therefore be carried out without affecting the IP_2 performance. The IM_3 response of the proposed circuit is also simulated, and it is found to be similar to the reference, that is, approximately -103 dBm (measured -96 dBm and -98 dBm for new concept and reference respectively) at 500 kHz for an input signal level of -30 dBm. The IIP_3 is also

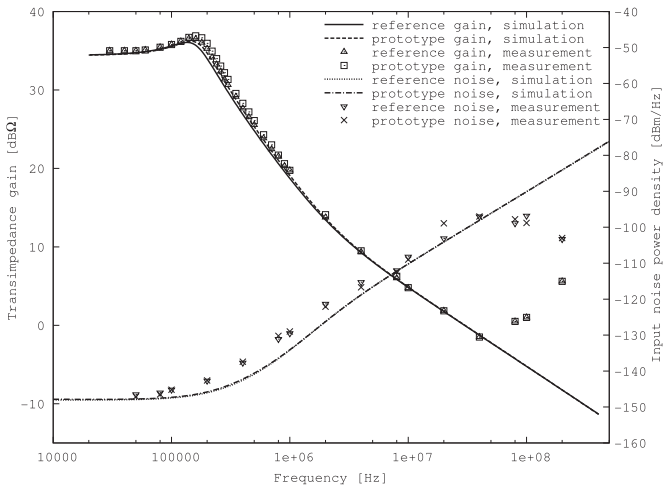

Fig. 12. Measured versus simulated transfer curves and input referred noise for the reference and prototype amplifiers.

TABLE I
COMPARISON BETWEEN IMMUNITY ENHANCEMENT APPROACHES

Source	Improvement	Frequency
source buffering [8]	14 dB	200 - 800 MHz
fully symmetrical topology [4]	> 20 dB	1 MHz - 4 GHz
filtered dummy stage [5]	18 dB	30 - 40 MHz
complementary differential pair [6]	18 dB	100 MHz
double differential stage [7]	60 dB	1 GHz
this work	31 dB	30 MHz

evaluated and found to be approximately -10 dBm for both circuits. The out-of-band interference immunity improvement obtained with the proposed method is compared to examples reported in the recent literature in Table I. In each case, the EMI susceptibility reduction is given relative to a circuit with a classical differential stage at the input. The frequency (range) of the improvement registered is also noted in the table. Source buffering [8] attempts to reduce the RFI-induced offset voltage at the common node of the differential pair. The other approaches [4]–[7] all aim to cancel distortion products at the output of the differential stage. The proposed method, on the other hand, modulates the voltage at the common node of the differential pair so that cancellation of the distortion products occurs throughout the circuit. While this comparison puts the current work in perspective, it should be noted that the IM_2 cancellation approach proposed in this work can be combined with many of the other methods to yield an even greater improvement in immunity to second-order intermodulation distortion.

V. CONCLUSION

When aiming for low-cost, fully integrated baseband amplifiers with minimal susceptibility to out-of-band interference signals (i.e., high IP_2), enhancements beyond classical differential design approaches must be considered. It was demonstrated in this paper that undesired local feedback of IM_2 products in a differential input stage degrades the robustness to out-of-band interference significantly, even when the stage has perfectly balanced outputs. For this reason, compensation of even-order distortion components is required at the input as well as the output of a differential stage. The design strategy

proposed in this work enables IP_2 compensation of practical differential amplifiers without compromising low-noise performance or other electrical parameters in the design space. The voltage headroom between supply rails is reduced slightly by resistive degeneration. A prototype circuit which demonstrates up to four orders of magnitude better immunity to out-of-band interference than the corresponding reference design was described in detail.

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